

Compal Confidential

Model Name : Q5LJ1(MA51-HX)

File Name : LA-8203P

BOM P/N:43

Compal Confidential

Q5LJ1 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH
Nvidia N13P-GS

2012-05-08

REV:1.0

| | | | | | |
|---|--------------------|-----------------|-------------------------------|-----------------------------|----------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/24 | Deciphered Date | 2012/07/12 | Title SCHEMATIC MB A8203 | |
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Fan Control
page 38

Nvidia
N13P GS
with GDDR5
page 22~28

PEG(DIS)

PCI-E 2.0x16 5GT/s PER LANE
CLK=100MHz

eDP(UMA/OPTIMUS)

Intel
Sandy/Ivy Bridge
ULV Processor
BGA1023
page 4~10

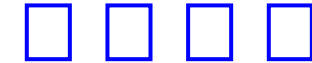
Memory BUS(DDRIII)
Dual Channel

204pin DDRIII-SO-DIMM X1

BANK 0, 1, 2, 3
page 11,12

1.5V DDRIII 1066/1333

DDRIII-ON BOARD 2G 1Rx16



HDMI Conn.
page 29

eDP Conn.
page 28

FDI x8

CLK=100MHz
2.7GT/s

DMI x4

CLK=100MHz
2.5GB/s x4

USB 3.0
conn x2
USB port 0,1
page 34

USB 2.0
conn x1
USB port 9
page 34

MINI Card
BT
USB port 8
page 36

CMOS
Camera
USB port 10
page 28

USBx14

3.3V 48MHz

HD Audio

3.3V 24MHz

SPI

LPC

HDA Codec
ALC271X-VB6
page 38

PCI-Express x 8 (PCI-E 2.0 5GT/s)

CLK=100MHz

port 1

port 2

port 3

SATA x 6 (GEN2 3.0GT/S, GEN3 6GT/S)

CLK=100MHz

LAN(GbE)
Boardcom
57780
page 34

MINI Card
WLAN
page 36

Card reader
page 35

GEN3
port 1

GEN3
port 0

GEN2
port 2

mSATA
MINI Card
USB port 12
page 33

SATA HDD
Conn.
page 30

SATA CDROM
Conn.
page 30

LPC BUS
CLK=33MHz

ENE
KB9012/KB930
page 35

Touch Pad
page 36

Int.KBD
page 36

EC ROM x1
(KB930)
page 36

RTC CKT.
page 13

Power On/Off CKT.
page 36

DC/DC Interface CKT.
page 39,40

Power Circuit DC/DC
page 41~53

LS-8201P
PWR/B
page 36

| | | | | | | |
|---|--------------------|-----------------|------------|-------------------------------|------------------------|-------|
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| | | | | Date: Thursday, June 14, 2012 | Sheet 2 of 56 | |

| Voltage Rails | | AC | AC | AC | AC | DC | DC | DC |
|--|---|------|------|------|-----|-----|-----|-----|
| Power Plane | Description | S0 | S3 | S4 | S5 | DS3 | DS4 | DS5 |
| +RTCVCC | RTC power | ON | ON | ON | ON | ON | ON | ON |
| VIN | Adapter power supply (19V) | N/A | ON | ON | ON | OFF | OFF | OFF |
| BATT+ | Battery power supply (12.6V) | N/A | N/A | N/A | N/A | ON | ON | ON |
| B+ | AC or battery power rail for power circuit. | ON | ON | ON | ON | ON | ON | ON |
| +VSB | +VSBP to +VSB always on power rail for sequence control | ON | ON | OFF | OFF | OFF | OFF | OFF |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +VGFX_CORE | Core voltage for UMA graphic | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +5VALW | +5VALWP to +5VALW power rail | ON | ON | ON | ON | ON | ON | ON |
| +5VALW_PCH | +5VALW to +5VALW_PCH power rail for PCH | ON | ON | ON | OFF | OFF | OFF | OFF |
| +5VS | +5VALW to +5VS switched power rail | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +3VALW | +3VALW always on power rail | ON | ON | ON | ON | ON | ON | ON |
| +3VALW_PCH | +3VALW to +3VALW_PCH power rail for PCH | ON | ON | ON | OFF | OFF | OFF | OFF |
| +3VS | +3VALW to +3VS power rail | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +VCCSA | +VCCSA POWER RAIL TO CPU | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +1.8VS | +3VALW to 1.8V switched power rail to PCH & GPU | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +1.5V | +1.5VP to +1.5V power rail for DDRIII | ON | ON | OFF | OFF | ON | OFF | OFF |
| +1.5VS | +1.5V to +1.5VS switched power rail | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +1.05VS_VTT | +1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +0.75VS | +0.75VP to +0.75VS switched power rail for DDR terminator | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| +3V_LAN | LAN CHIP POWER RAIL | ON | ON | ON | ON | OFF | OFF | OFF |
| +3VS_WLAN | WLAN MODULE POWER RAIL | ON | OFF* | OFF* | OFF | OFF | OFF | OFF |
| +USB3_VCCA | USB SLEEP CHARGER & PORT0 POWER POWER RAIL | ON* | ON | ON | ON | ON* | ON* | ON* |
| +USB3_VCCB/C | USB PORT1/9 POWER POWER RAIL | ON | ON | OFF | OFF | OFF | OFF | OFF |
| +3VSDGPU | +3VS to +3VSDGPU power rail | ON** | OFF | OFF | OFF | OFF | OFF | OFF |
| +VGA_CORE | Core voltage for GPU | ON** | OFF | OFF | OFF | OFF | OFF | OFF |
| +1.5VSDGPU | +1.5V to +1.5VSDGPU switched power rail for GPU | ON** | OFF | OFF | OFF | OFF | OFF | OFF |
| +1.05VSDGPU | +1.05VSDGPU switched power rail for GPU | ON** | OFF | OFF | OFF | OFF | OFF | OFF |
| Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF | | | | | | | | |
| Note : ON** Depend on Optimus ON/OFF. | | | | | | | | |
| Note : OFF* Depend on IOAC SPEC support or not. | | | | | | | | |

| EC SM Bus1 address | | EC SM Bus2 address | |
|--------------------|-------------|-------------------------|------------|
| Device | Address | Device | Address |
| Smart Battery | 0001 011X b | On Board Thermal Sensor | 1001_101xb |

PCH SM Bus address

| Device | Address |
|----------|-------------------------------|
| ChannelA | DIMM0 A0 1010 000X |
| ChannelB | DIMM0 A4 1010 010X |
| | JDIMM1(SPD) On Board RAM(SPD) |

CPU BOM Config

| | | | | |
|---------|----------|----|------|--|
| I32367@ | I3-2367M | HR | 1.4G | SA000051H60 (S IC AV8062701047904 SR0CV J1 1.4G ABOI) |
| I32377@ | I3-2377M | HR | 1.5G | SA00005MX10 (S IC AV8062701048004 QAXQ J1 1.5G BGA) |
| I52467@ | I5-2467M | HR | 1.6G | SA00004X010 (S IC AV8062701047504 SR0D6 J1 1.6G ABOI) |
| | | | | |
| I33217@ | I3-3217U | CR | 1.8G | SA00005L5C0(S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO I) |
| I53317@ | I5-3317U | CR | 1.7G | SA00005K6B0(S IC AV8063801058002 SR0N8 L1 1.7G ABOI) |
| I73517@ | I7-3517U | CR | 1.9G | SA00005K5B0(S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO I) |

GPU BOM Config + GPIO

| | | |
|------------|----|--|
| N13P-GS-A2 | R3 | SA0000518A0 (S IC N13P-GS-A2 FCBGA 908P GPU ABO I) |
|------------|----|--|

VRAM BOM Config

| | | | | | | |
|--------------|--------|-------|-------|----|--|----------|
| X76364BOL03: | 1G HYN | GDDR5 | 64*32 | 2G | SA00004GD30(S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABOI) | HYNMFR@/ |
| X76364BOL04: | 1G HYN | GDDR5 | 64*32 | 2G | SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABOI) | HYNAFR@/ |

RAM BOM Config

| | | | | | | |
|--------------|--------------|--------|-----|------|--|----------------|
| X76364BOL11: | 2GB*4 HYNIX | HYNIX | 2GB | 1333 | SA00005FV10(S IC D3 256MX16/1333 H5TC4G63MFR-H9A FBGA 96P ABO I) | RAM@//HYNIX@/ |
| X76364BOL12: | 2GB*4 ELPDIA | ELPDIA | 2GB | 1333 | SA000059110(S IC D3 256M16 EDJ4216EBBG-DJ-F ABOI) | RAM@//ELPIDA@/ |

BOM Config

| | | |
|------------------|-------------------------|-------------|
| LA8203 UMA : | 9012@/UMAO@/DRAM@/ | +CPU config |
| LA8203 Optimus : | 9012@/DIS@/DRAM@/VRAM@/ | +CPU config |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| | | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| Full ON | | | | | | | | | |
| S1(Power On Suspend) | | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

Board ID / SKU ID Table for AD channel

| Vcc | 3.3V +/- 5% | | | |
|----------|--------------|-------------|-------------|-------------|
| Ra/Rc/Re | 100K +/- 5% | | | |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0 | |
| 1 | |
| 2 | 0.1 |
| 3 | 0.2 |
| 4 | 1.0 |
| 5 | |
| 6 | |
| 7 | |

USB Port Table

| USB 2.0 | Port | 3 External USB Port |
|---------|------|---------------------------------|
| EHCI1 | 0 | USB Port(Right 2.0),USB Charger |
| | 1 | USB Port(Mid 2.0) |
| | 2 | |
| | 3 | |
| | 4 | |
| | 5 | |
| | 6 | |
| EHCI2 | 7 | |
| | 8 | BT (WLAN) |
| | 9 | USB port(Left 2.0) |
| | 10 | Camera |
| | 11 | Mini Card(MSATA) |
| | 12 | |
| | 13 | |

| USB 3.0 | Port | |
|---------|------|---------------------|
| XHCI | 1 | USB Port(Right 3.0) |
| | 2 | USB Port(Mid 3.0) |
| | 3 | |
| | 4 | |

| BTO Option Table | |
|------------------|---------------|
| BTO Item | BOM Structure |
| Unpop | @ |
| EC 9012 | 9012@ |
| EC 930 | 930@ |
| Connector | CONN@ |
| ALC281 | 281@ |
| UMA Only | UMAO@ |
| OPT | DIS@ |
| HR CPU I3-2367M | I32367 @ |
| HR CPU I3-2377M | I32377 @ |
| HR CPU I5-2467M | I52467 @ |
| CR CPU I3-3217M | I33217 @ |
| CR CPU I5-3317M | I53317 @ |
| CR CPU I7-3517M | I73517 @ |
| GDDR5 HYNIX MFR | HYNMFR@ |
| GDDR5 HYNIX AFR | HYNAFR@ |
| DRAM | RAM@ |
| DRAM HYNIX | HYNIX@ |
| DRAM ELPIDA | ELPIDA@ |
| VRAM X76 | VRAM@ |
| DRAM X76 | DRAM@ |

P.56
P.56
P.56

P.56
P.56
P.56

X76364BOL03 P.27
X76364BOL04 P.27
for X76 RAM GPIO P.18
for X76364BOL11: P.56
for X76364BOL12: P.56
MB VRAM X76 P.56
MB DRAM X76 P.56

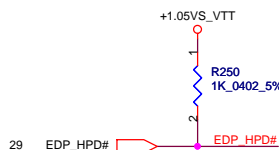
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| | | | | Date: | Thursday, June 14, 2012 |
| | | | | Sheet | 3 of 56 |

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms can't be left floating ,even if disable eDP function...

Add eDP circuit



15 DMI_CRX_PTX_N0
15 DMI_CRX_PTX_N1
15 DMI_CRX_PTX_N2
15 DMI_CRX_PTX_N3
15 DMI_CRX_PTX_P0
15 DMI_CRX_PTX_P1
15 DMI_CRX_PTX_P2
15 DMI_CRX_PTX_P3
15 DMI_CTX_PRX_N0
15 DMI_CTX_PRX_N1
15 DMI_CTX_PRX_N2
15 DMI_CTX_PRX_N3
15 DMI_CTX_PRX_P0
15 DMI_CTX_PRX_P1
15 DMI_CTX_PRX_P2
15 DMI_CTX_PRX_P3

M2 DMI_RX#[0]
P6 DMI_RX#[1]
P10 DMI_RX#[3]
N3 DMI_RX#[0]
P7 DMI_RX#[1]
P3 DMI_RX#[2]
P11 DMI_RX#[3]
K1 DMI_TX#[0]
M8 DMI_TX#[1]
N4 DMI_TX#[2]
R2 DMI_TX#[3]
K3 DMI_TX#[0]
M7 DMI_TX#[1]
P4 DMI_TX#[2]
T3 DMI_TX#[3]

15 FDI_CTX_PRX_N0
15 FDI_CTX_PRX_N1
15 FDI_CTX_PRX_N2
15 FDI_CTX_PRX_N3
15 FDI_CTX_PRX_N4
15 FDI_CTX_PRX_N5
15 FDI_CTX_PRX_N6
15 FDI_CTX_PRX_N7
15 FDI_CTX_PRX_P0
15 FDI_CTX_PRX_P1
15 FDI_CTX_PRX_P2
15 FDI_CTX_PRX_P3
15 FDI_CTX_PRX_P4
15 FDI_CTX_PRX_P5
15 FDI_CTX_PRX_P6
15 FDI_CTX_PRX_P7

U7 FDI0_TX#[0]
W11 FDI0_TX#[1]
W1 FDI0_TX#[2]
AA6 FDI0_TX#[3]
W6 FDI0_TX#[0]
V4 FDI0_TX#[1]
Y2 FDI0_TX#[2]
AC9 FDI0_TX#[3]
U6 FDI0_TX#[0]
W10 FDI0_TX#[1]
W3 FDI0_TX#[2]
AA7 FDI0_TX#[3]
W7 FDI0_TX#[0]
T4 FDI0_TX#[1]
AA3 FDI0_TX#[2]
AC8 FDI0_TX#[3]

15 FDI_FSYNCO
15 FDI_FSYNC1
15 FDI_INT
15 FDI_LSYNCO
15 FDI_LSYNC1

AA11 FDI0_FSYNCO
AC12 FDI0_FSYNC1
U11 FDI_INT
AA10 FDI0_LSYNCO
AG8 FDI0_LSYNC1

W=12mil L=500mil S=15mil

EDP_COMP
EDP_HPDI#

29 EDP_AUXN
29 EDP_AUXP

AG4 eDP_AUX#
AF4 eDP_AUX

29 EDP_TXN0
29 EDP_TXP0

AC3 eDP_TX#[0]
AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]
AC1 eDP_TX#[0]
AA4 eDP_TX#[1]
AE10 eDP_TX#[2]
AE6 eDP_TX#[3]

UCPU1A

DMI

Intel(R) iGPU

PCI EXPRESS -- GRAPHICS

eDP

IVY-BRIDGE_BGA1023

W=12mil L=500mil S=15mil

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO

PEG_RX#[0] H22 PEG GTX C HRX N15 C262 1
PEG_RX#[1] J21 PEG GTX C HRX N14 C244 1
PEG_RX#[2] B22 PEG GTX C HRX N13 C264 1
PEG_RX#[3] D21 PEG GTX C HRX N12 C246 1
PEG_RX#[4] A19 PEG GTX C HRX N11 C267 1
PEG_RX#[5] D17 PEG GTX C HRX N10 C248 1
PEG_RX#[6] B14 PEG GTX C HRX N9 C268 1
PEG_RX#[7] D13 PEG GTX C HRX N8 C250 1
PEG_RX#[8] A11 PEG GTX C HRX N7 C270 1
PEG_RX#[9] B10 PEG GTX C HRX N6 C252 1
PEG_RX#[10] A8 PEG GTX C HRX N4 C254 1
PEG_RX#[11] B6 PEG GTX C HRX N3 C274 1
PEG_RX#[12] H8 PEG GTX C HRX N2 C257 1
PEG_RX#[13] E5 PEG GTX C HRX N1 C276 1
PEG_RX#[14] K7 PEG GTX C HRX N0 C259 1
PEG_RX#[15]

PEG_RX#[0] K22 PEG GTX C HRX P15 C263 1
PEG_RX#[1] K19 PEG GTX C HRX P14 C245 1
PEG_RX#[2] C21 PEG GTX C HRX P13 C265 1
PEG_RX#[3] D19 PEG GTX C HRX P12 C247 1
PEG_RX#[4] C19 PEG GTX C HRX P11 C266 1
PEG_RX#[5] D16 PEG GTX C HRX P10 C249 1
PEG_RX#[6] D12 PEG GTX C HRX P8 C251 1
PEG_RX#[7] C11 PEG GTX C HRX P7 C271 1
PEG_RX#[8] C9 PEG GTX C HRX P6 C253 1
PEG_RX#[9] F8 PEG GTX C HRX P5 C273 1
PEG_RX#[10] C8 PEG GTX C HRX P4 C255 1
PEG_RX#[11] C5 PEG GTX C HRX P3 C275 1
PEG_RX#[12] H6 PEG GTX C HRX P2 C256 1
PEG_RX#[13] F6 PEG GTX C HRX P1 C277 1
PEG_RX#[14] K6 PEG GTX C HRX P0 C258 1
PEG_RX#[15]

PEG_TX#[0] G22 PEG HTX GRX N15 C597 1
PEG_TX#[1] C23 PEG HTX GRX N14 C578 1
PEG_TX#[2] D23 PEG HTX GRX N13 C594 1
PEG_TX#[3] F21 PEG HTX GRX N12 C574 1
PEG_TX#[4] H19 PEG HTX GRX N11 C593 1
PEG_TX#[5] C17 PEG HTX GRX N10 C572 1
PEG_TX#[6] K15 PEG HTX GRX N9 C591 1
PEG_TX#[7] F17 PEG HTX GRX N8 C570 1
PEG_TX#[8] E14 PEG HTX GRX N7 C589 1
PEG_TX#[9] A15 PEG HTX GRX N6 C568 1
PEG_TX#[10] J14 PEG HTX GRX N5 C587 1
PEG_TX#[11] H13 PEG HTX GRX N4 C566 1
PEG_TX#[12] M10 PEG HTX GRX N3 C584 1
PEG_TX#[13] F10 PEG HTX GRX N2 C564 1
PEG_TX#[14] D9 PEG HTX GRX N1 C582 1
PEG_TX#[15] J4 PEG HTX GRX N0 C562 1

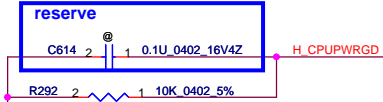
PEG_TX#[0] F22 PEG HTX GRX P15 C596 1
PEG_TX#[1] A23 PEG HTX GRX P14 C575 1
PEG_TX#[2] D24 PEG HTX GRX P13 C595 1
PEG_TX#[3] E21 PEG HTX GRX P12 C573 1
PEG_TX#[4] G19 PEG HTX GRX P11 C592 1
PEG_TX#[5] B18 PEG HTX GRX P10 C571 1
PEG_TX#[6] K17 PEG HTX GRX P9 C590 1
PEG_TX#[7] G17 PEG HTX GRX P8 C569 1
PEG_TX#[8] E14 PEG HTX GRX P7 C588 1
PEG_TX#[9] C15 PEG HTX GRX P6 C567 1
PEG_TX#[10] K13 PEG HTX GRX P5 C586 1
PEG_TX#[11] G13 PEG HTX GRX P4 C565 1
PEG_TX#[12] K10 PEG HTX GRX P3 C585 1
PEG_TX#[13] G10 PEG HTX GRX P2 C563 1
PEG_TX#[14] D8 PEG HTX GRX P1 C583 1
PEG_TX#[15] K4 PEG HTX GRX P0 C561 1

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

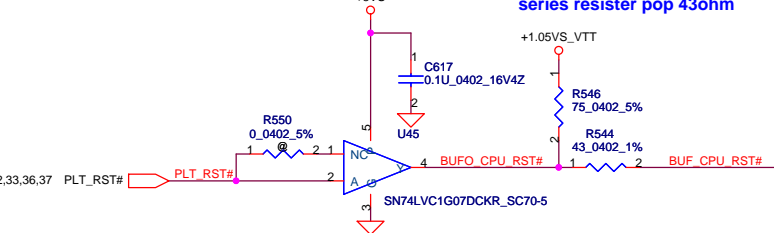
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| Date: | Thursday, June 14, 2012 | Sheet | 4 | of | 56 |

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0

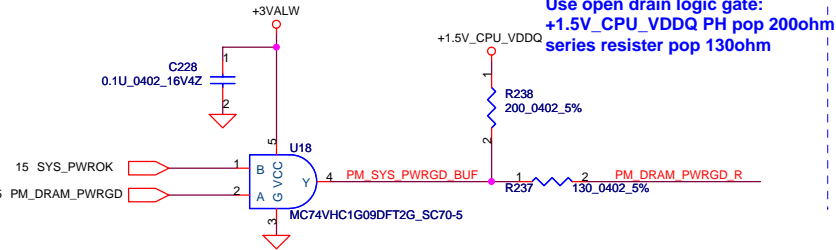


Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU



RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0



PROC_SELECT#
PH VCPLL and connect to PCH DF_TV5

偵測CPU有無安裝

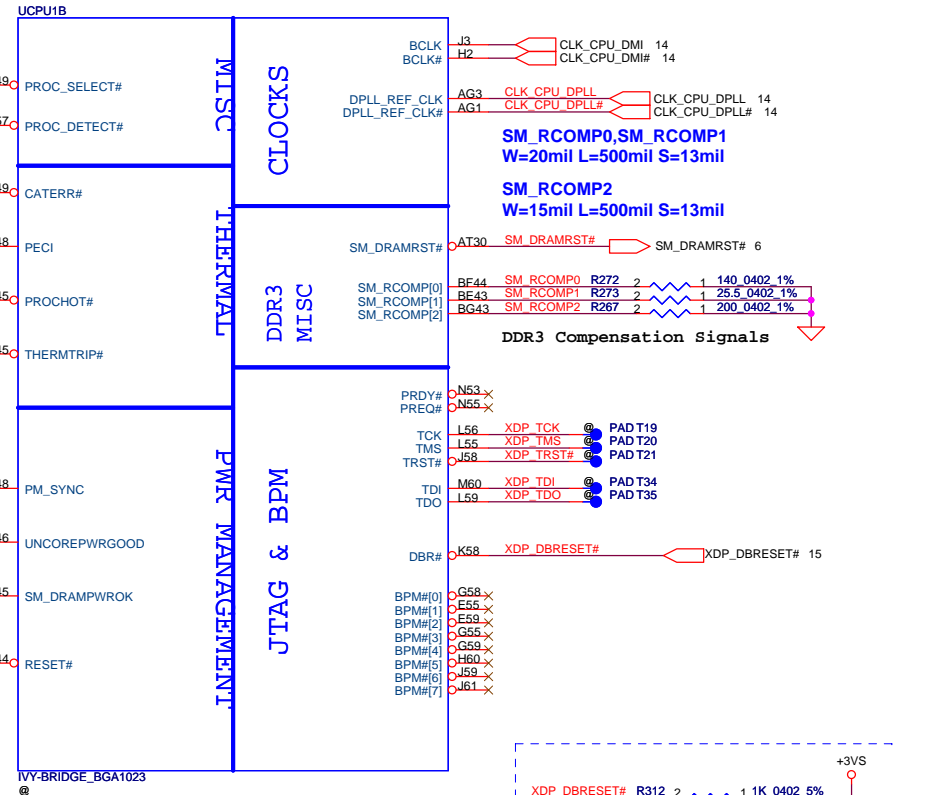
XBOX 三紅功能

follow Checklist 1.5

18 H_THRMTRIP#

UNCOREPWRGOOD:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok



0921 LVDS@->@

CLK_CPU_DPLL# R517 2 1K_0402_5%
CLK_CPU_DPLL R516 2 1K_0402_5%
Checklist1.5 P.67 Graphis Disable Guide
DIS only SKU eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

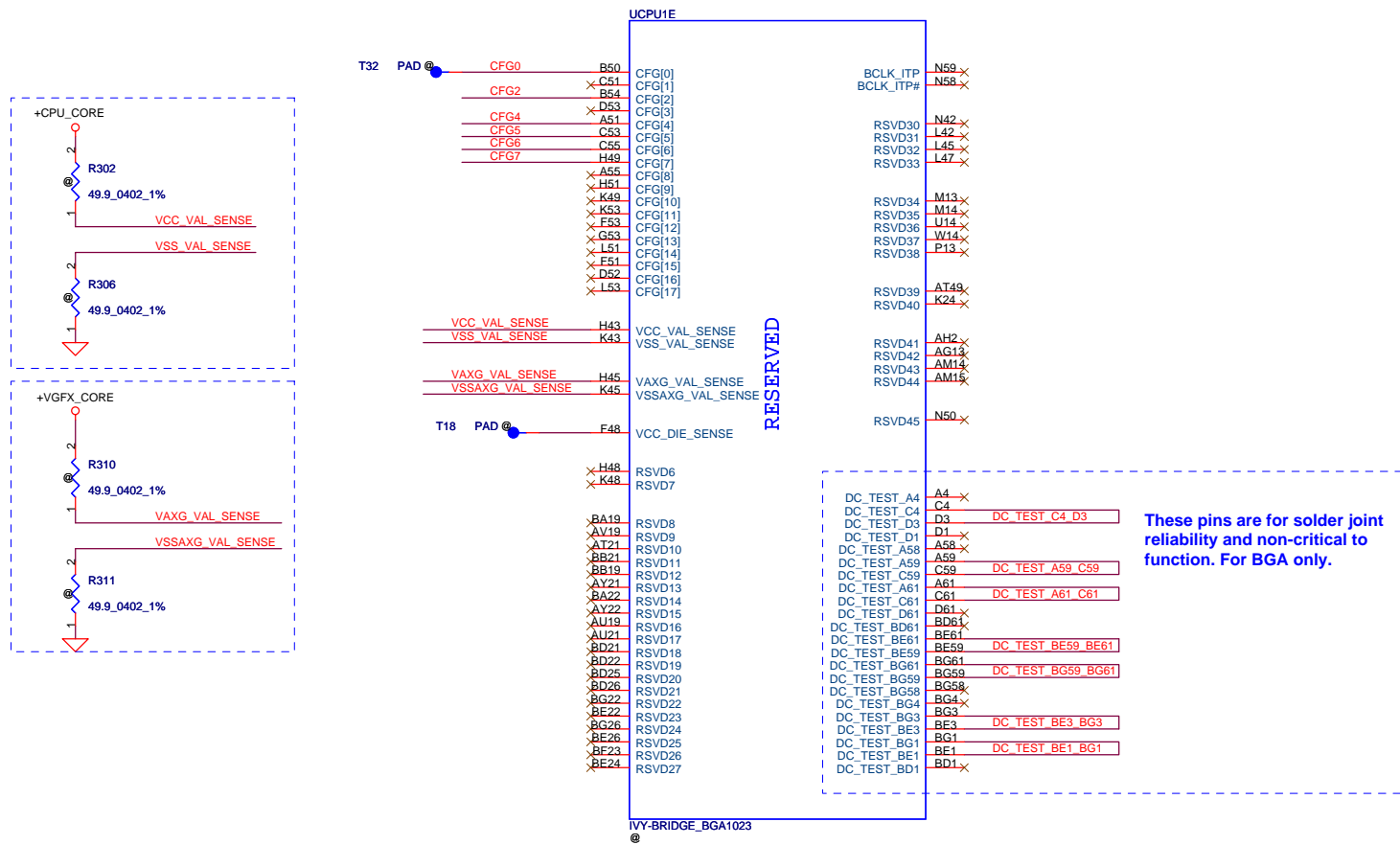
SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

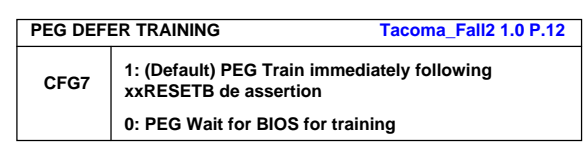
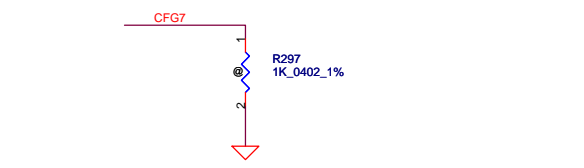
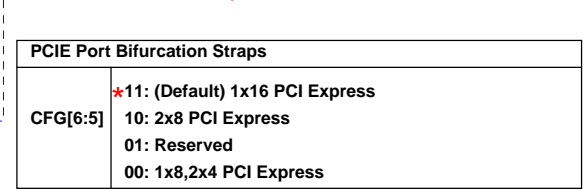
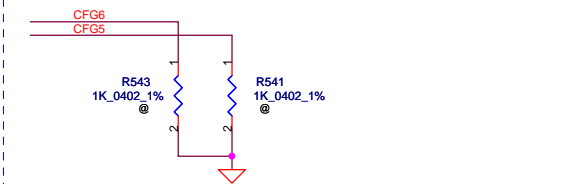
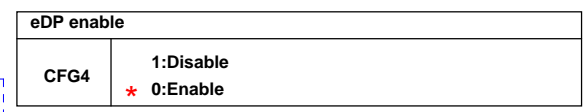
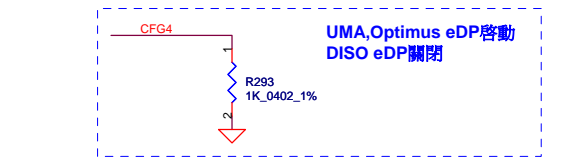
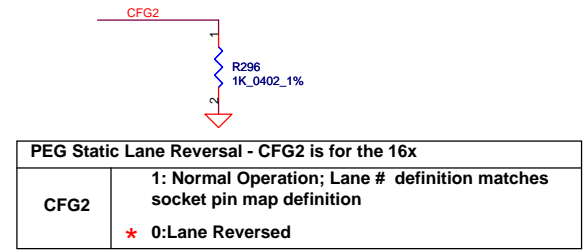
DDR3 Compensation Signals

Tacoma_Fall2 1.0 PH 1K +3VS
Check list 1.5 PH 1K +3VS
Debug port DG1.1-1.3 50-5K ohm

| | | | | | | |
|---|--------------------|-----------------|------------|-------------------------------|------------------------|-------|
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| | | | | Date: Thursday, June 14, 2012 | Sheet 5 of 56 | |



CFG Straps for Processor



INTEL Recommend VCC
4*470uF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

INTEL Recommend VCCIO
2*330uF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

POWER

ULV type
DC 33A

UCPU1F

8.5A

+CPU_CORE

+1.05VS_VTT

CORE SUPPLY

PEG IO AND DDR IO

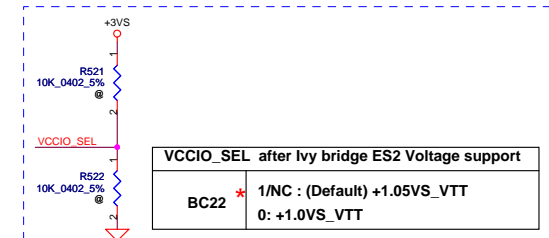
QUIET
RAILS

SVID

SENSE LINES

For DDR

For PEG



Place the PU
resistors close to CPU

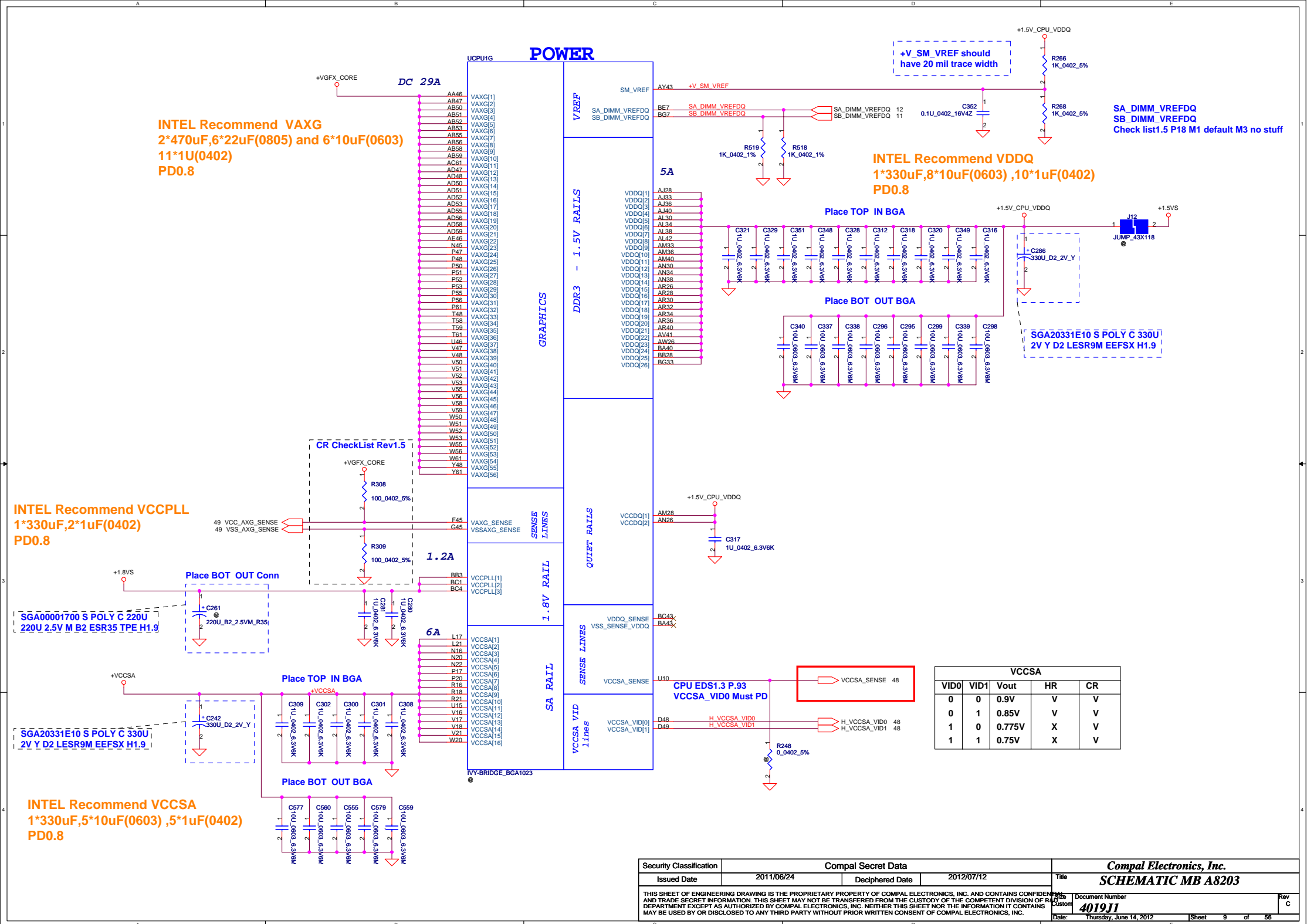
Place the PU
resistors close to VR

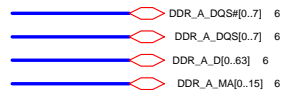
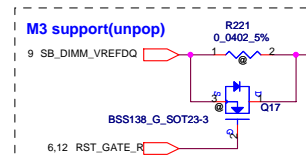
Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

Check list 1.5

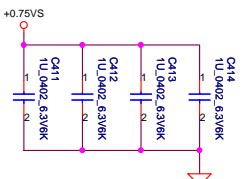
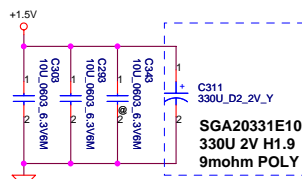
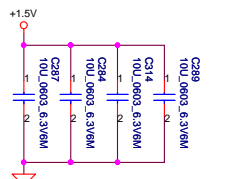
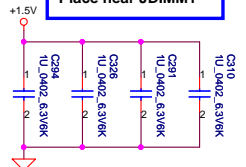
IVY-BRIDGE_BGA1023

| | | | | |
|--|--------------------|-----------------|--------------------------|-------------------------------|
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| | | | | Rev |
| | | | | C |
| | | | | Date: Thursday, June 14, 2012 |
| | | | | Sheet 8 of 56 |





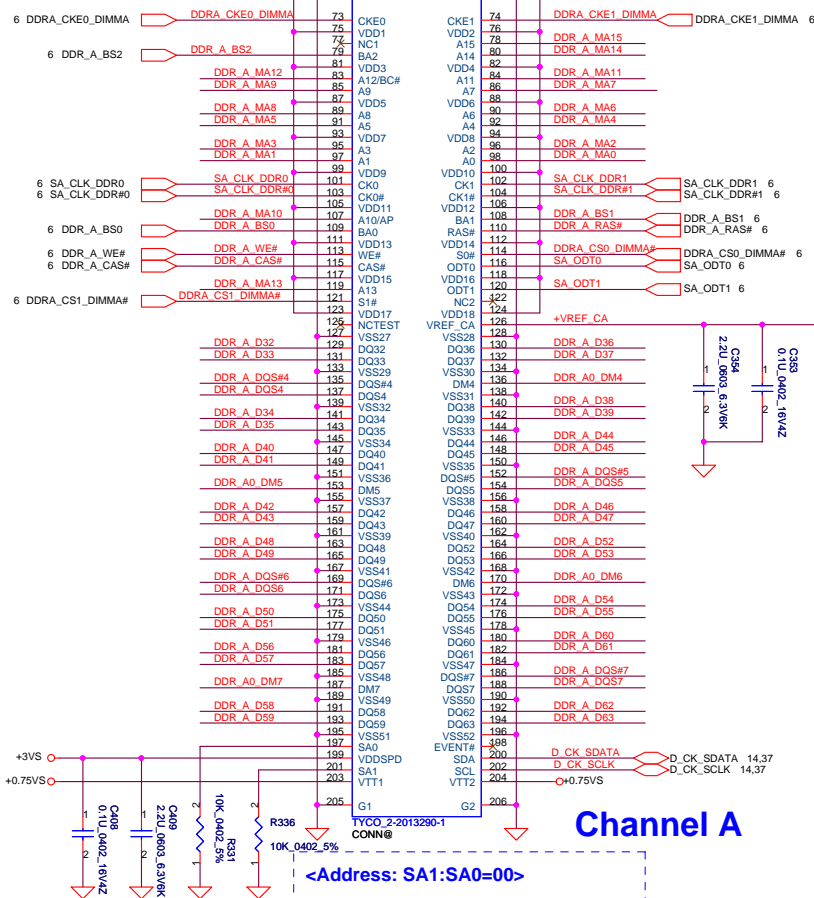
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



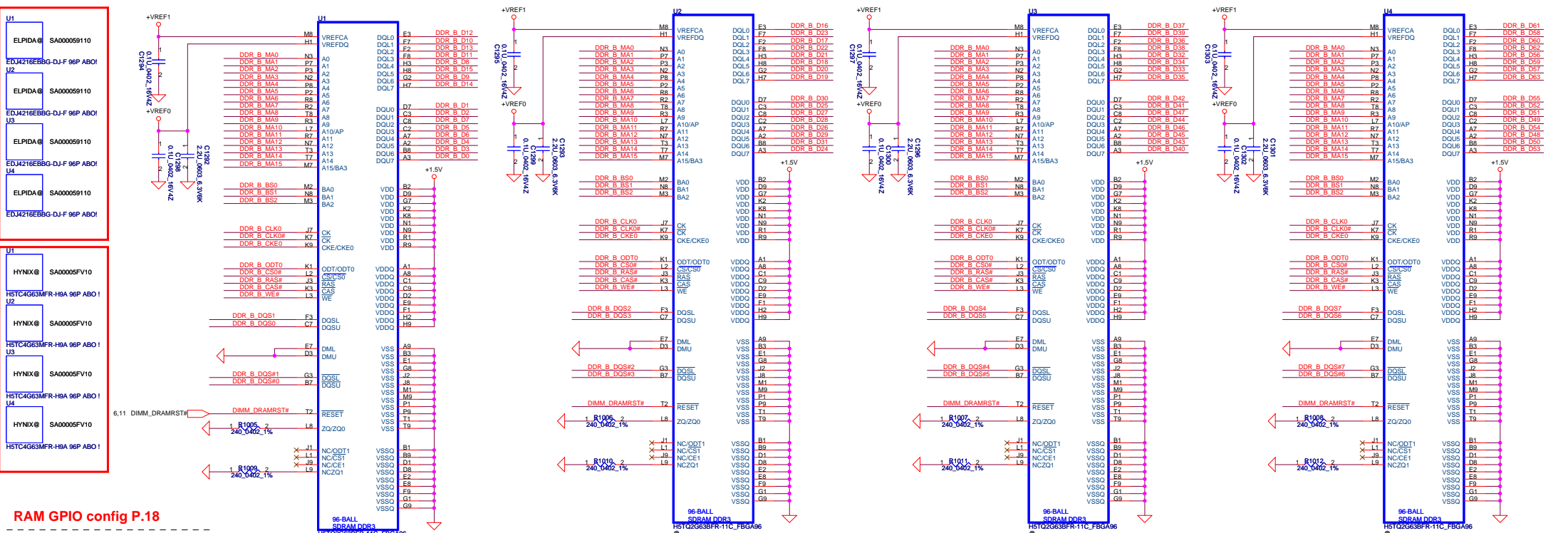
All VREF traces should have 10 mil trace width



Channel A

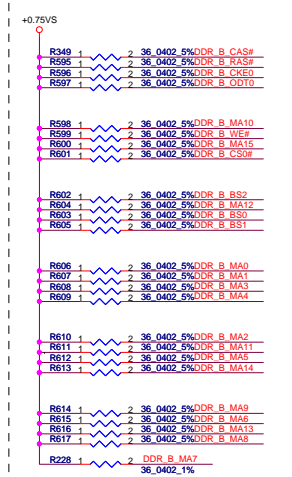
<Address: SA1:SA0=00>
DIMM_1 Reverse H:5.2mm

| | | | | | |
|--|--|---|--|--------------------------|--|
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| 401911 | | Rev | | C | |
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RAM GPIO config P.18

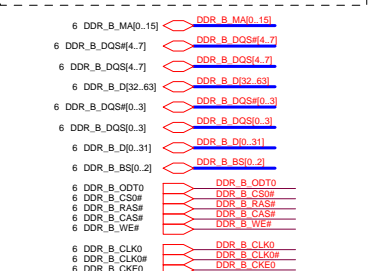
DDR3 CTL/ADD Termination



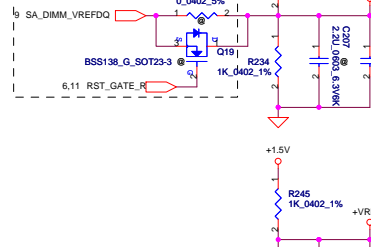
DDR3 CLK Termination

1.CAD Note: Cterm= 1.6pF should be kept near feeding point of first SDRAM

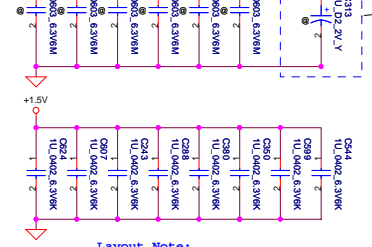
2.CAD Note: Rtt= 30.1ohms, Ctt= 0.1uF should be kept within 600mils from last SDRAM

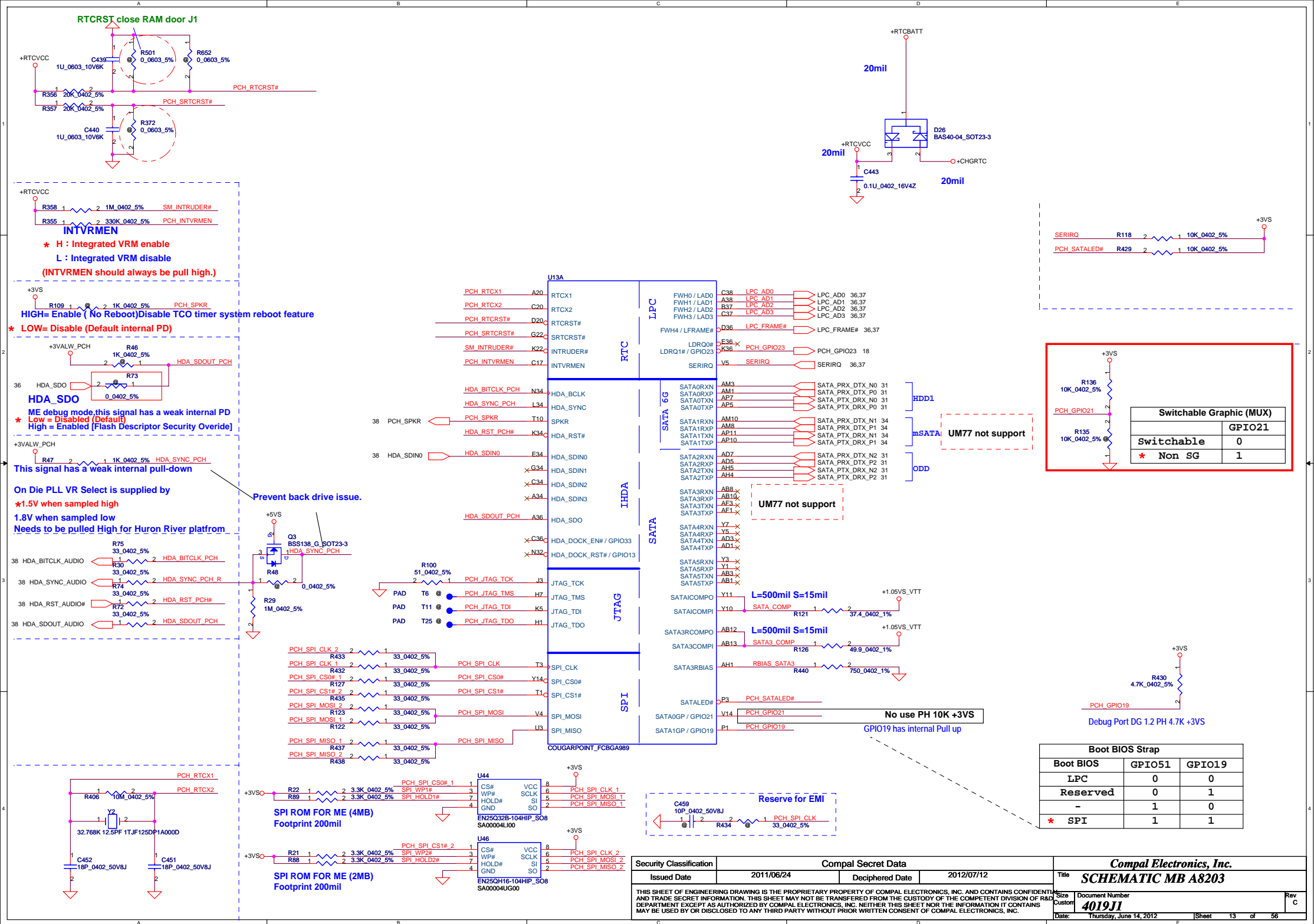


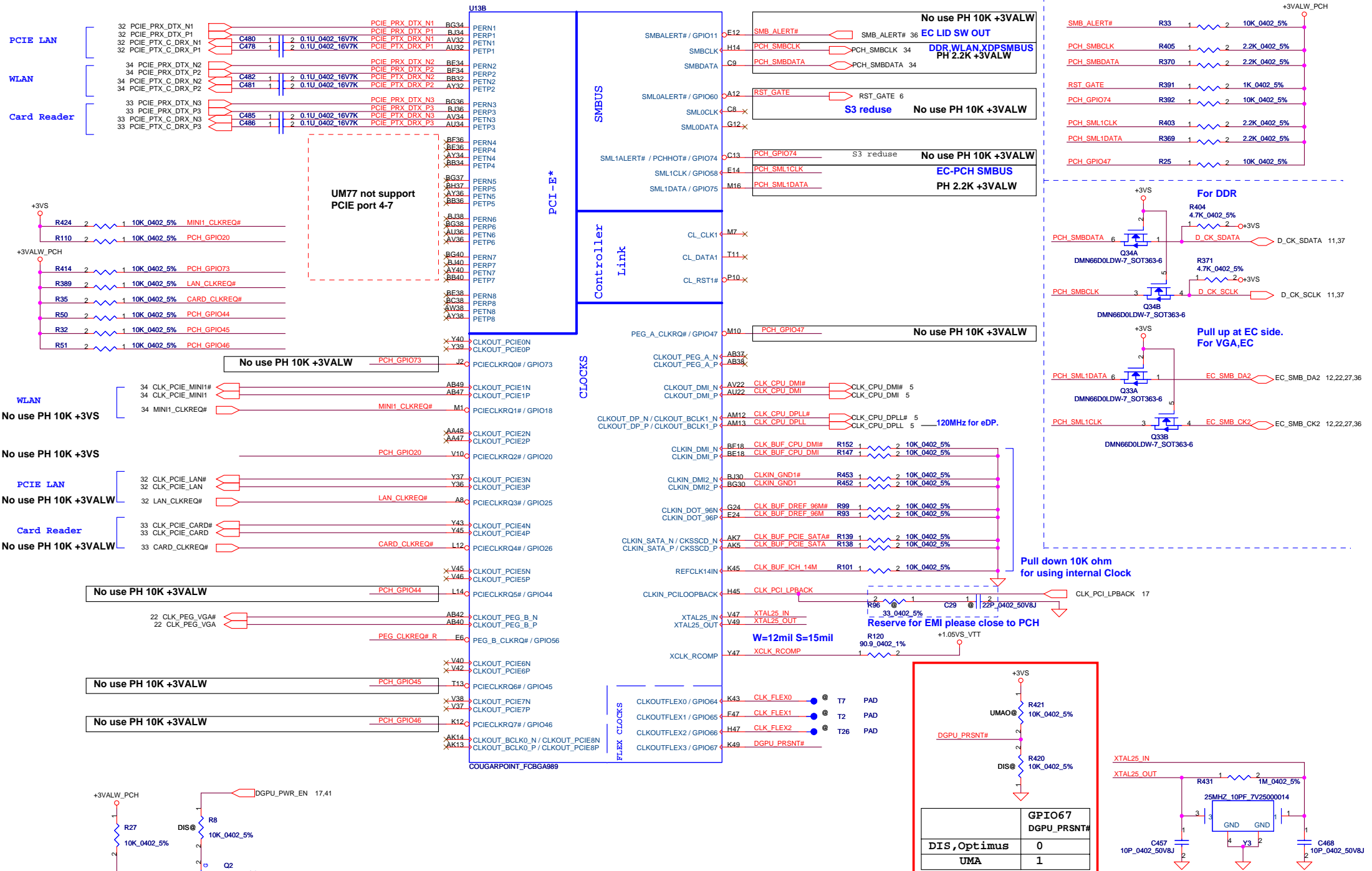
External DDR Thermal Sensor

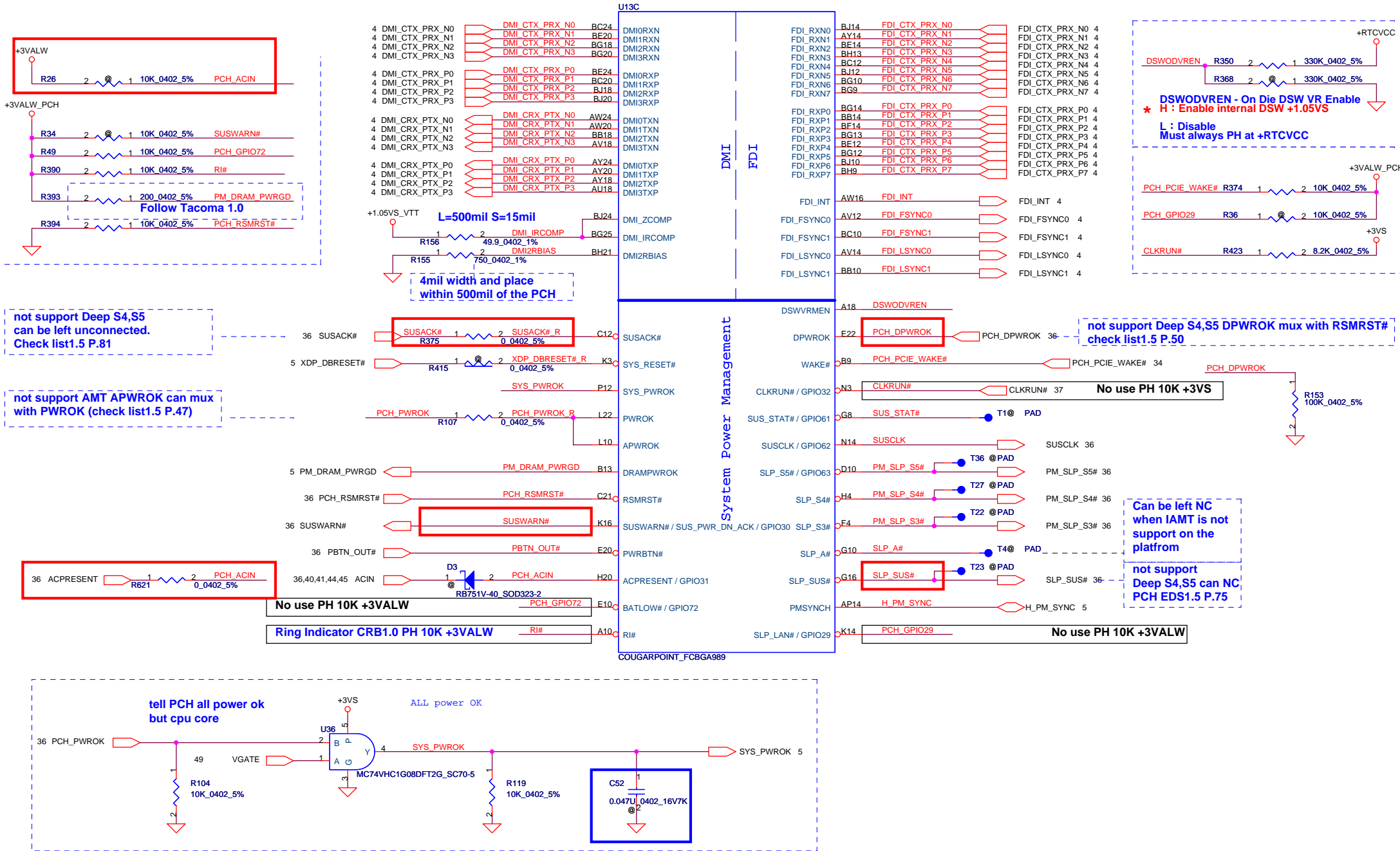


Layout Note: Place near each memory part







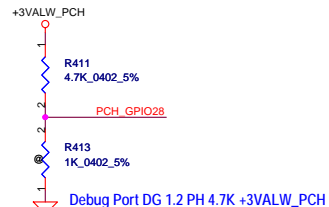


HDA_SYNC PH(PLL =+1.5VS)

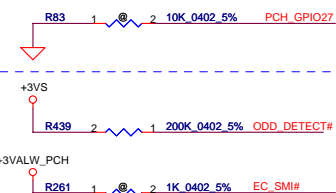
GPIO28

On-Die PLL Voltage Regulator

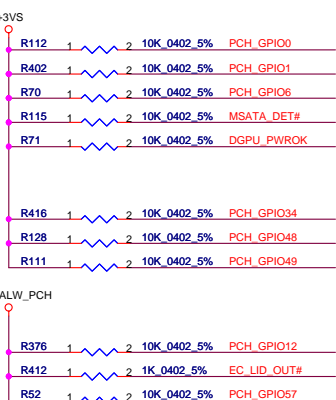
This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 * L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37
 Sampled at Rising edge of PWROK.
 Weak internal pull-down.
 (weak internal pull-down is disabled
 after PLTRST# de-asserts)
 NOTE: This signal should NOT be
 pulled high when strap is sampled



GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration
 register bits are not cleared by
 CF9h reset event.
 CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs
 TACH1-7 only on server
 can insted to GPIO

| | | |
|-------------------------------------|----------------------------|-----|
| No use PH 10K +3VS | PCH_GPIO0 | TZ |
| No use PH 10K +3VS | PCH_GPIO1 | A42 |
| No use PH 10K +3VS | PCH_GPIO6 | H36 |
| No use PH 10K +3VS | 36 EC_SCI# | E38 |
| No use PH 10K +3VALW | 36 EC_SMI# | C10 |
| No use PH +3VALW | PCH_GPIO12 | C4 |
| No use PH +3VALW | 36 EC_LID_OUT# | G2 |
| No use PH +3VS | 34 MSATA_DET# | U2 |
| No use PH +3VS | 50 VGA_PWROK | D40 |
| No use PH 10K +3VS | RAM flag | T5 |
| No use PH +3VALW | DDR3/DDR3L | E8 |
| No use PD 10K to GND | PCH_GPIO27 | E16 |
| No use PH 10K +3VALW | PCH_GPIO28 | P8 |
| No use PH 10K +3VS | BT ON/OFF | K1 |
| No use can NC | PAD T12 @ | K4 |
| Can't PH | 31 ODD_DETECT# | V8 |
| Can't PH | PAD T10 @ | K4 |
| No use PH 10K +3VS | Optimus(L)/ non optimus(H) | N2 |
| No use PH 10K +3VS | RAM flag | M3 |
| No use PH 10K +3VS | PCH_GPIO48 | V13 |
| SATA5GP&TEMP_ALERT# CRB PH 10K +3VS | PCH_GPIO49 | V3 |
| No use PH +3VALW | PCH_GPIO57 | D6 |

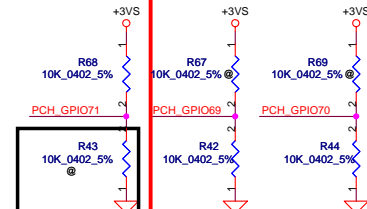
| | |
|------------|-------------|
| UMAO@ | GPIO38 |
| DIS@ | OPTIMUS_EN# |
| * Muxless | 0 |
| nonMuxless | 1 |

| | |
|---------|------------|
| DDR3L | GPIO24 |
| DDR3 | PCH_GPIO24 |
| * DDR3L | 0 |
| DDR3 | 1 |

GPIO36/GPIO37 is Strap functionality
 that requires internal pull down to be sampled at rising PWROK.
 When uses as SATA2GP/SATA3GP for mechanical presence detect
 -use a external pull up 150K-200K ohm to Vcc3_3
 When used as GP input
 -ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP
 -use 8.2K-10K pull-down
 check list page 47

12/19 modify

| | |
|-------|--------|
| GDDR5 | GPIO71 |
| GDDR3 | 1 |
| GDDR3 | 0 |



| Project ID | | GPIO69 | GPIO70 |
|------------|---|--------|--------|
| * | X | 0 | 0 |
| | X | 0 | 1 |
| | X | 0 | 1 |
| | X | 1 | 0 |
| | X | 0 | 0 |
| | X | 0 | 1 |
| | X | 0 | 1 |
| | X | 1 | 0 |
| | X | 1 | 1 |
| | X | 1 | 0 |
| | X | 1 | 1 |

GPIO

CPU/MISC

NCTF

TACH4 / GPIO68
 TACH5 / GPIO69
 TACH6 / GPIO70
 TACH7 / GPIO71

LAN_PHY_PWR_CTRL / GPIO12
 GPIO15

SATA4GP / GPIO16
 TACH0 / GPIO17

SCLOCK / GPIO22
 GPIO24 / MEM_LED

GPIO27
 GPIO28

STP_PC# / GPIO34
 GPIO35

SATA2GP / GPIO36
 SATA3GP / GPIO37

SLOAD / GPIO38
 SDATAOUT0 / GPIO39

SDATAOUT1 / GPIO48
 SATA5GP / GPIO49

GPIO57

VSS_NCTF_15
 VSS_NCTF_16

VSS_NCTF_17
 VSS_NCTF_18

VSS_NCTF_19
 VSS_NCTF_20

VSS_NCTF_21
 VSS_NCTF_22

VSS_NCTF_23
 VSS_NCTF_24

VSS_NCTF_25
 VSS_NCTF_26

VSS_NCTF_27
 VSS_NCTF_28

VSS_NCTF_29
 VSS_NCTF_30

VSS_NCTF_31
 VSS_NCTF_32

ODD_EN#
 PCH_GPIO69
 PCH_GPIO70
 PCH_GPIO71

PECI
 RCIN#
 PROCWGRD
 THRMTRIP#

INIT3_3V#
 AH8
 AK11
 AH10
 AK10
 P37

TS_VSS1-4
 PD to GND

9/15 Layout
 request remove
 Test point
 They will route
 by itself

9/15 Layout
 request remove
 Test point
 They will route
 by itself

9/15 Layout
 request remove
 Test point
 They will route
 by itself

9/15 Layout
 request remove
 Test point
 They will route
 by itself

9/15 Layout
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9/15 Layout
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9/15 Layout
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 They will route
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9/15 Layout
 request remove
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 They will route
 by itself

9/15 Layout
 request remove
 Test point
 They will route
 by itself

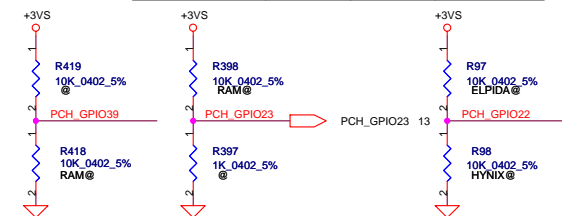
9/15 Layout
 request remove
 Test point
 They will route
 by itself

9/15 Layout
 request remove
 Test point
 They will route
 by itself

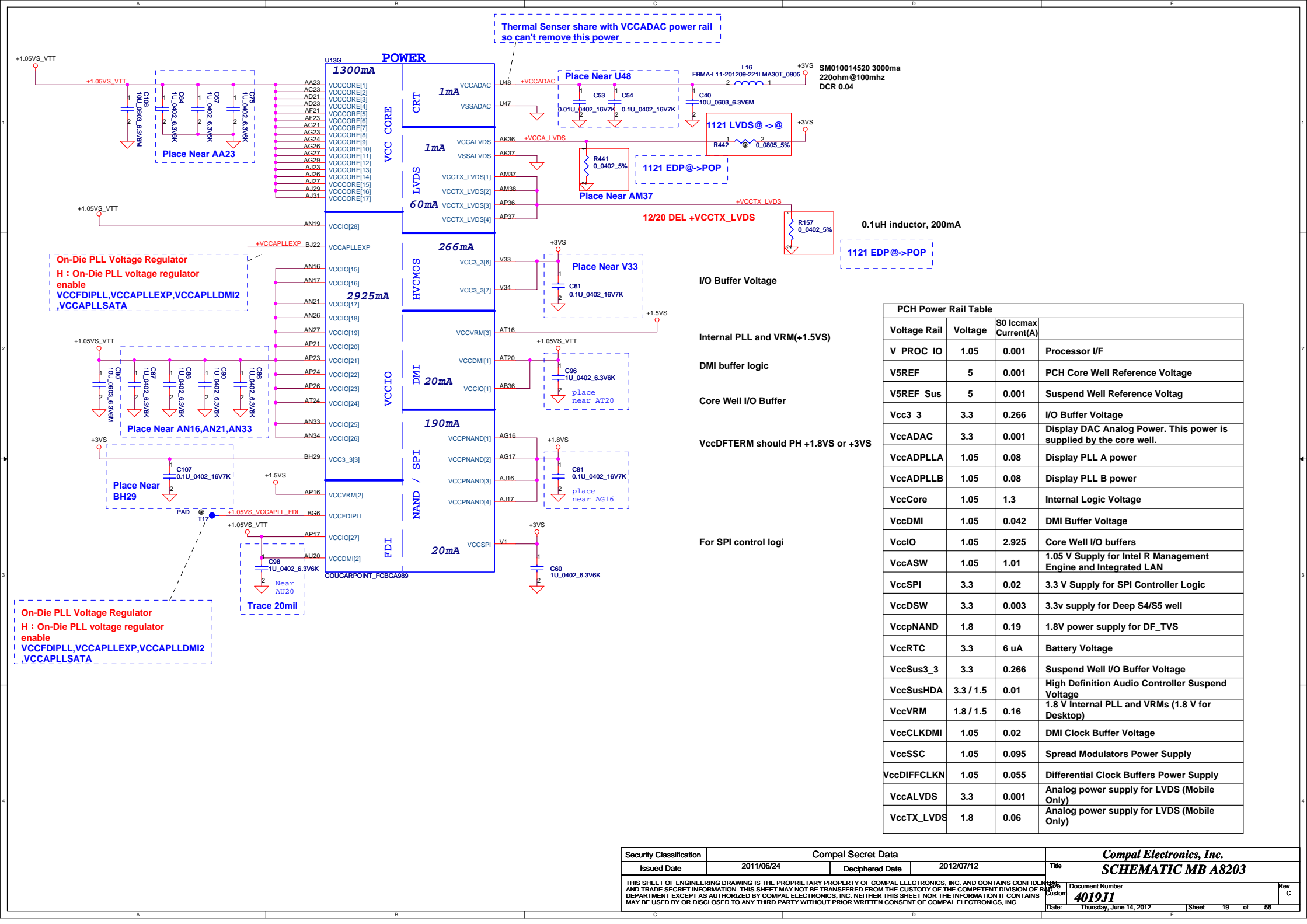
PECI CPU-EC
 CTRL+ALT+DEL
 non CPU power ok
 130c shut down



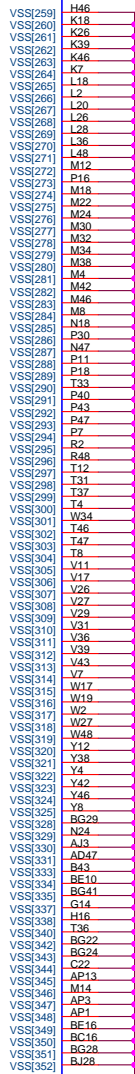
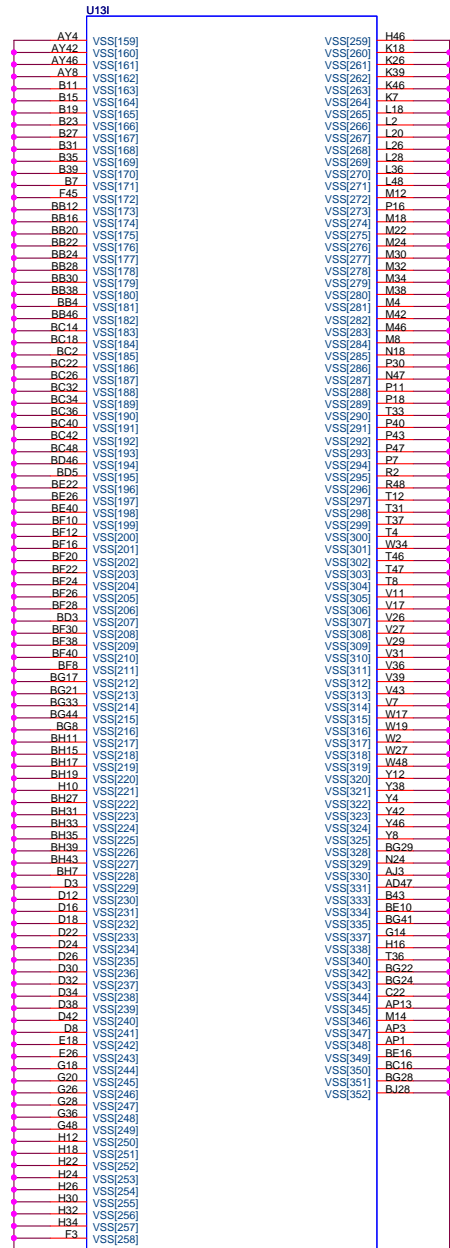
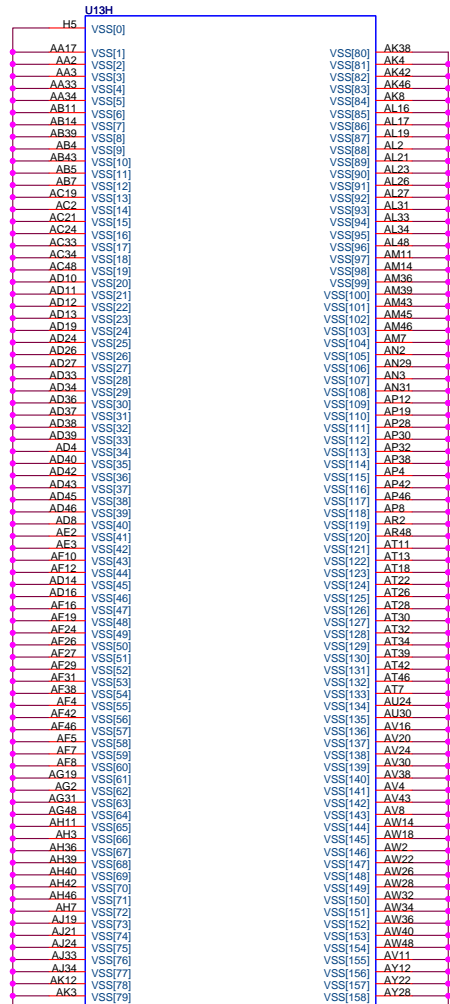
| on board ram flag | GPIO39 | GPIO23 | GPIO22 |
|-------------------|--------|--------|--------|
| EVT MICRON 4G | 0 | 0 | 0 |
| EVT ELPIDA 4G | 0 | 0 | 1 |
| DVT HYNIX 2G | 0 | 1 | 0 |
| DVT ELPIDA 2G | 0 | 1 | 1 |

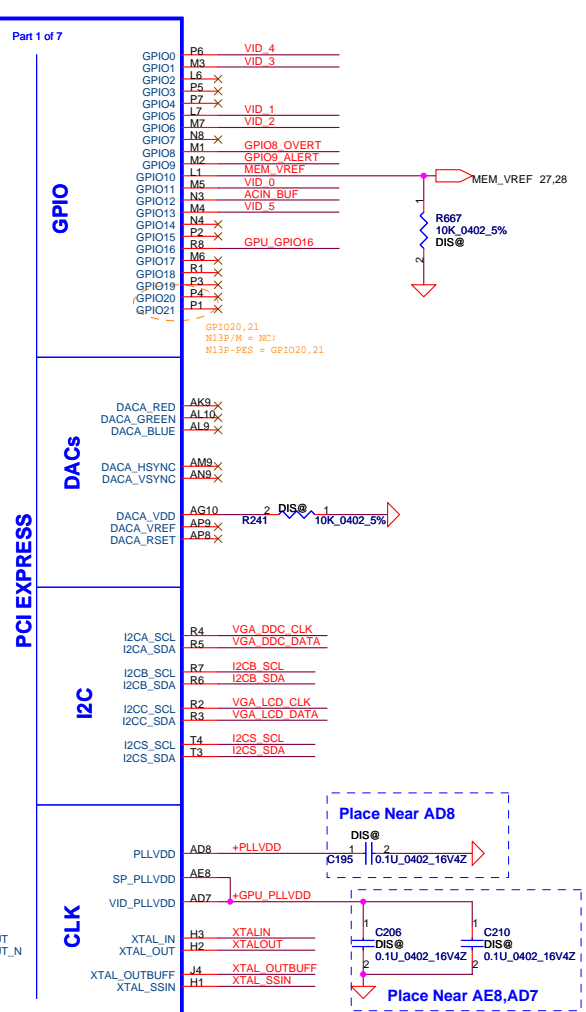
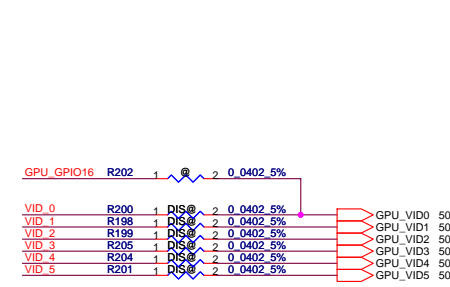
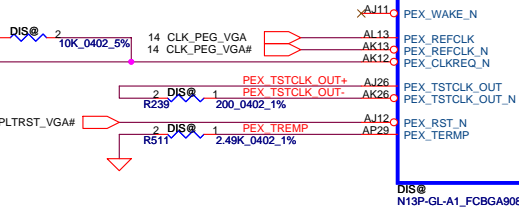
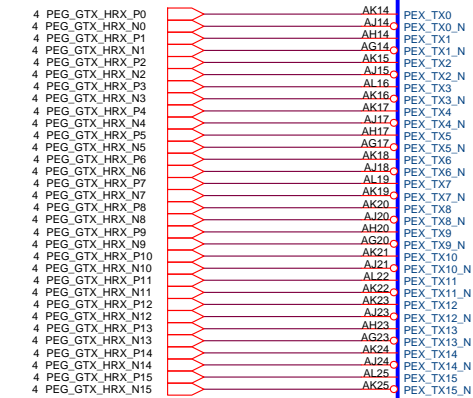
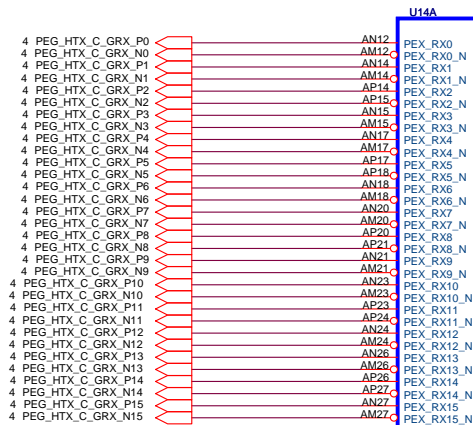


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| | | | | Sheet | 18 of 56 |





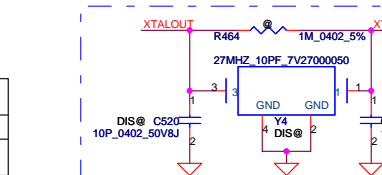
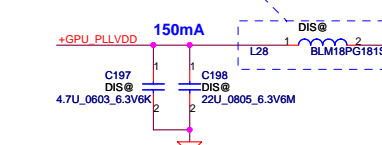
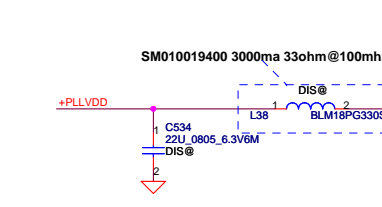
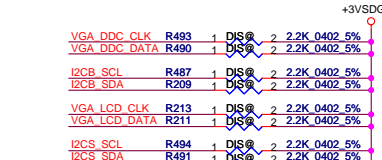
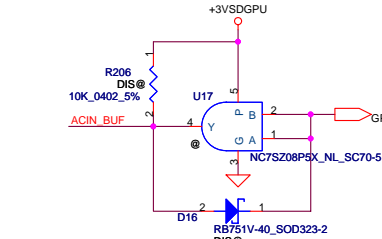
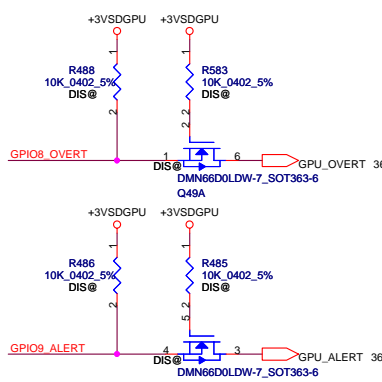




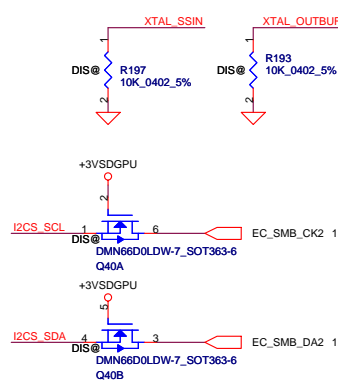
NV DG PLL_VDD
0.1Ux1
22Ux1 33ohm(ESR0.05)x1

NV DG SP_PLLVDD,VID_PLLVDD
0.1Ux2 Under GPU
4.7Ux1,22Ux1
180ohm(ESR0.2)x1

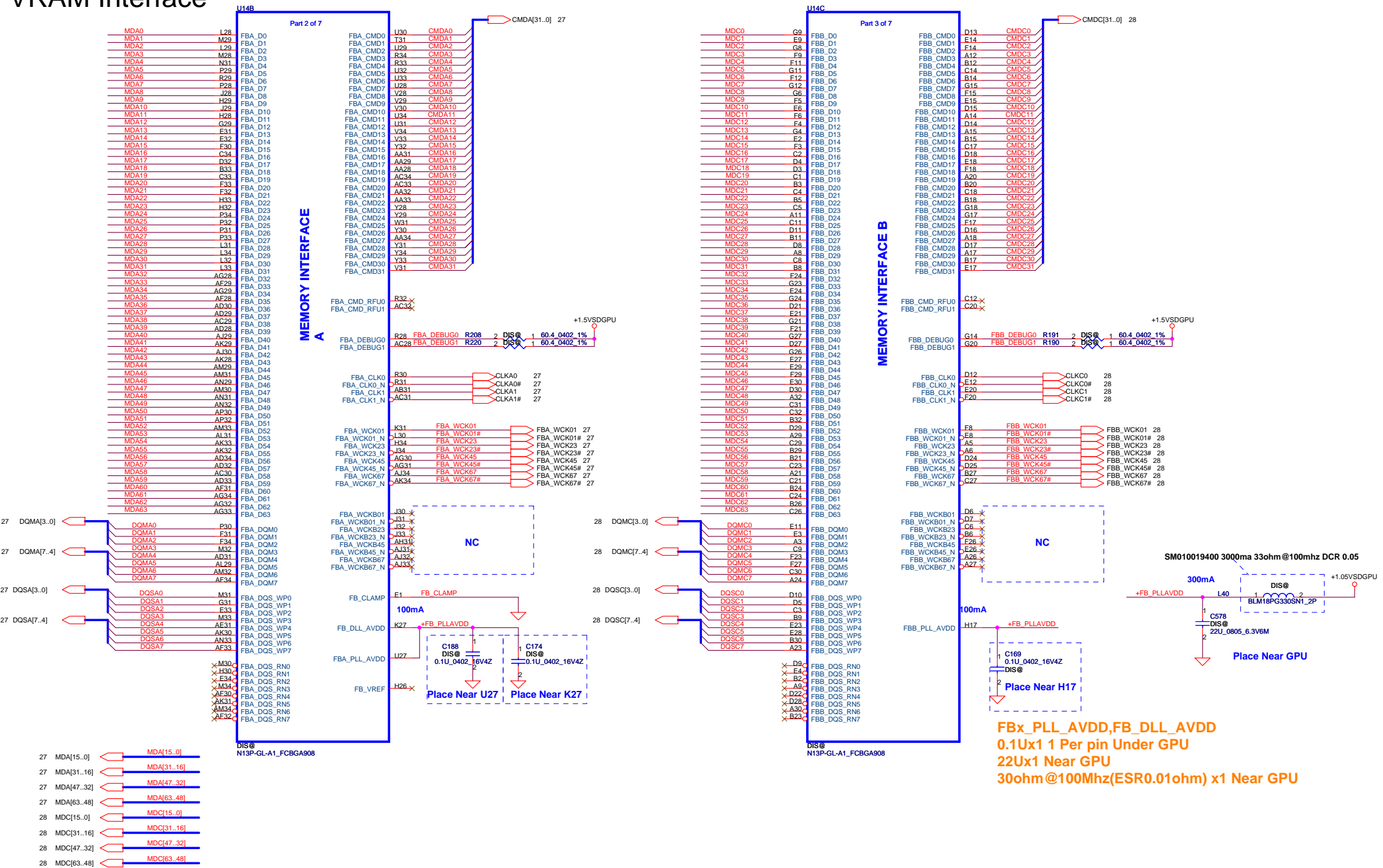
| VGA Chipset | Default | VID0 | VID1 | VID2 | VID3 | VID4 | VID5 | VID6 |
|---------------|---------|------|------|------|------|------|------|------|
| N13P-GS 29*29 | TBD | | | | | | | |
| N13P-GV 29*29 | 0.9V | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| N13M-GS 29*29 | | | | | | | | |



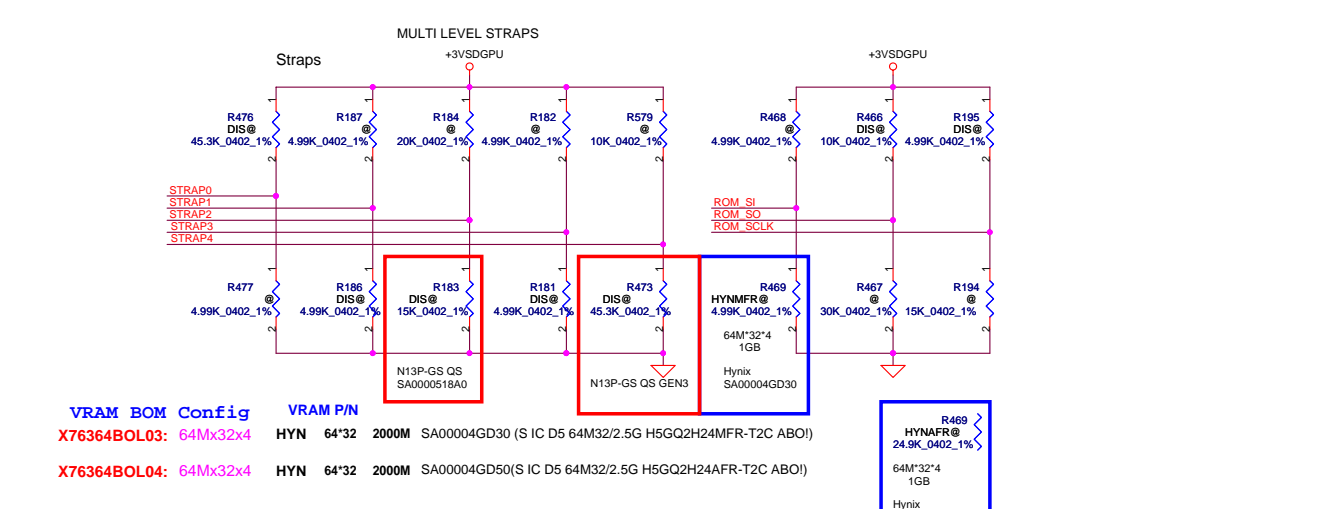
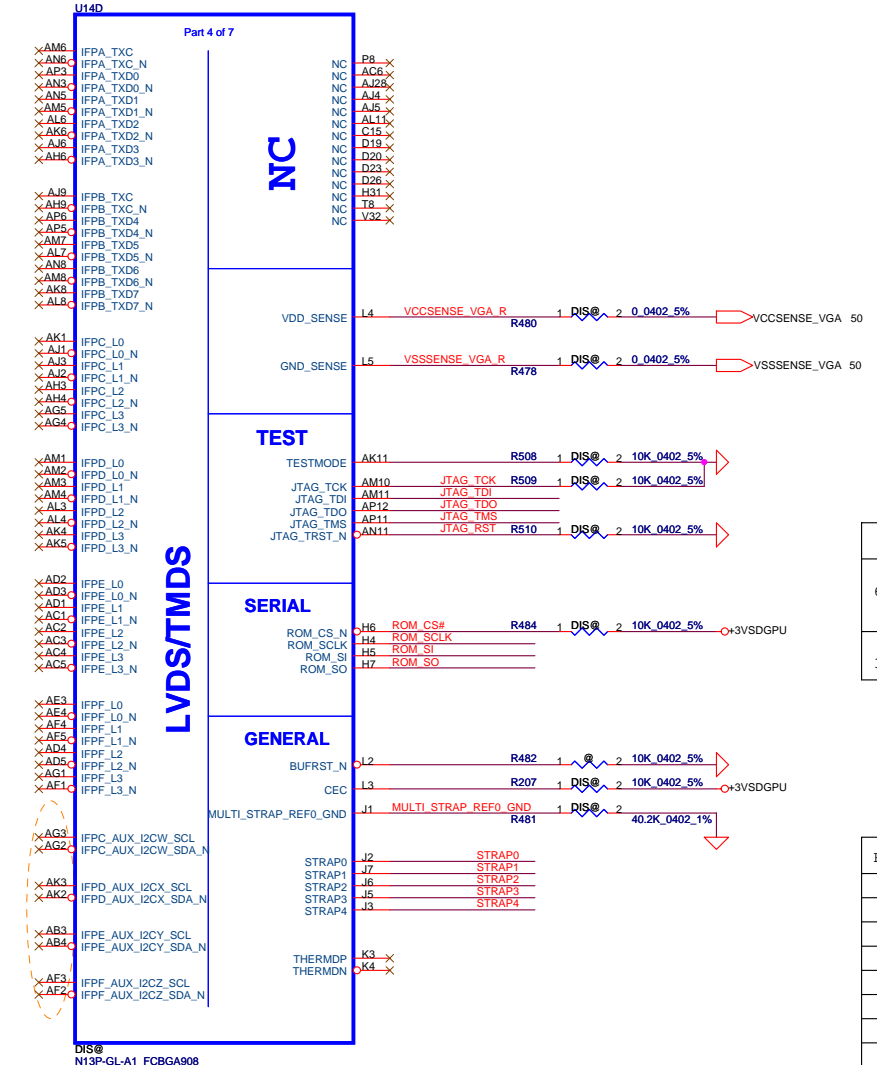
| GPIO | I/O | USAGE |
|--------|-----|---|
| GPIO0 | O | GPU_VID4 |
| GPIO1 | O | GPU_VID3 |
| GPIO2 | O | LCD_BL_PWM |
| GPIO3 | O | LCD_VCC |
| GPIO4 | O | LCD_BLEN |
| GPIO5 | O | GPU_VID1 |
| GPIO6 | O | GPU_VID2 |
| GPIO7 | O | 3D Vision |
| GPIO8 | I/O | OVERT |
| GPIO9 | I/O | ALERT |
| GPIO10 | O | MEM_VREF_CTL |
| GPIO11 | O | MEM_VDD_CTL(PES) GPU_VID0(Real N13P) |
| GPIO12 | I | PWR_LEVEL |
| GPIO13 | O | THERM_LOAD_STEP_DOWN |
| GPIO14 | I | HPD_AB |
| GPIO15 | I | HPD_C |
| GPIO16 | O | THERM_LOAD_STEP_UP |
| GPIO17 | I | HPD_D |
| GPIO18 | I | HPD_E |
| GPIO19 | I | HPD_F |
| GPIO20 | | Reserved |
| GPIO21 | | Reserved |
| GPIO22 | I/O | SLI_RASTER_SYNC |
| GPIO23 | O | SLI_SWAPRDY |
| GPIO24 | | |



VRAM Interface



| | | | | | | |
|--|--------------------|-----------------|------------|--------------------------|--------------------|-------|
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| | | | | Custom | 4019JI | C |
| Date: Thursday, June 14, 2012 | | | | Sheet | 23 | of 56 |



| GDDR5 | Vendor | Strap | ROM_SI |
|----------|----------|-------|--------|
| 64M x 32 | Hynix(M) | Ox0 | PD 5K |
| | Samsung | Ox1 | PD 10K |
| | Hynix(A) | Ox4 | PD 25K |
| 32M x 32 | Hynix | Ox2 | PD 15K |
| | Samsung | Ox3 | PD 20K |

For N13P-GS-A1(ES2) A2(QS) strap table Decive ID : 0x0FD2

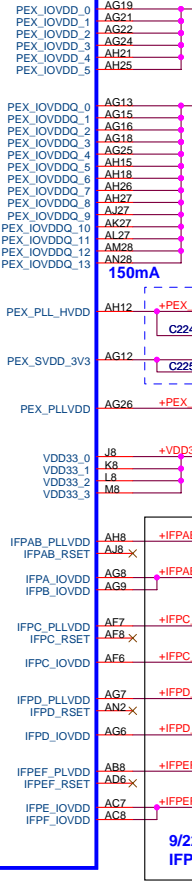
| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|----------|----------------|-------------------|----------|---------|----------|---------|----------|----------|---------|----------|
| N13P-GS | 2000 MHZ | 64M* 32* 4 1GB | Hynix SA00004GD30 | | | | | | R PD 5K | | |
| N13P-GS | 2000 MHZ | 64M* 32* 4 1GB | Samsung | R PU 45K | R PD 5K | R PD 15K | R PD 5K | R PD 45K | R PD 10K | R PU 5K | R PU 5K |
| N13P-GS | 2000 MHZ | 64M* 32* 4 1GB | Hynix SA00004GD50 | | | | | | R PD 25K | | |

| Resistor Values | Pull-up to +3V | Pull-down to Gnd |
|-----------------|----------------|------------------|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

| | |
|----------|---|
| STRAP0 | USER[3:0] |
| STRAP1 | 3GIO_PADCFG_LUT_ADR[3:0] |
| STRAP2 | PCI_DEVID[3:0] |
| STRAP3 | SOR[3:0] |
| STRAP4 | PEX_MAX_SPEED, DP_PLLVDD33V |
| ROM_SCLK | PCI_DEV[4:5], SUB_VENDOR, PEX_PLL_EN_TERM |
| ROM_SI | RAM_CFG[3:0] |
| ROM_SO | FB_BAR_SIZE[1:0], SMB_ALT_ADOOR, VGA_DEVICE |

| U14E | Part 5 of 7 |
|-----------|-------------|
| FBVDDQ_0 | |
| FBVDDQ_1 | |
| FBVDDQ_2 | |
| FBVDDQ_3 | |
| FBVDDQ_4 | |
| FBVDDQ_5 | |
| FBVDDQ_6 | |
| FBVDDQ_7 | |
| FBVDDQ_8 | |
| FBVDDQ_9 | |
| FBVDDQ_10 | |
| FBVDDQ_11 | |
| FBVDDQ_12 | |
| FBVDDQ_13 | |
| FBVDDQ_14 | |
| FBVDDQ_15 | |
| FBVDDQ_16 | |
| FBVDDQ_17 | |
| FBVDDQ_18 | |
| FBVDDQ_19 | |
| FBVDDQ_20 | |
| FBVDDQ_21 | |
| FBVDDQ_22 | |
| FBVDDQ_23 | |
| FBVDDQ_24 | |
| FBVDDQ_25 | |
| FBVDDQ_26 | |
| FBVDDQ_27 | |
| FBVDDQ_28 | |
| FBVDDQ_29 | |
| FBVDDQ_30 | |
| FBVDDQ_31 | |
| FBVDDQ_32 | |
| FBVDDQ_33 | |

PEX_SVDD/PLL_HVDD c0.1Ux1,4.7Ux2 Near GPU

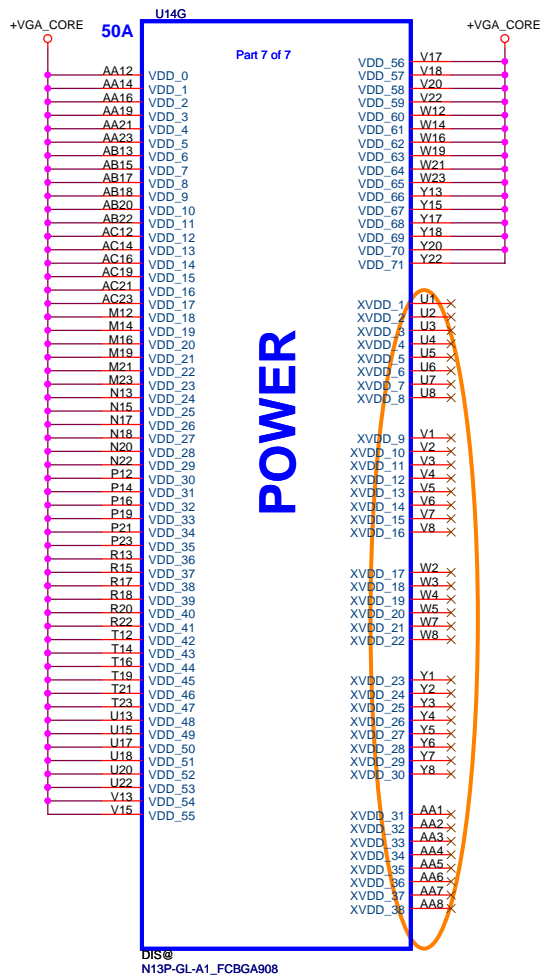
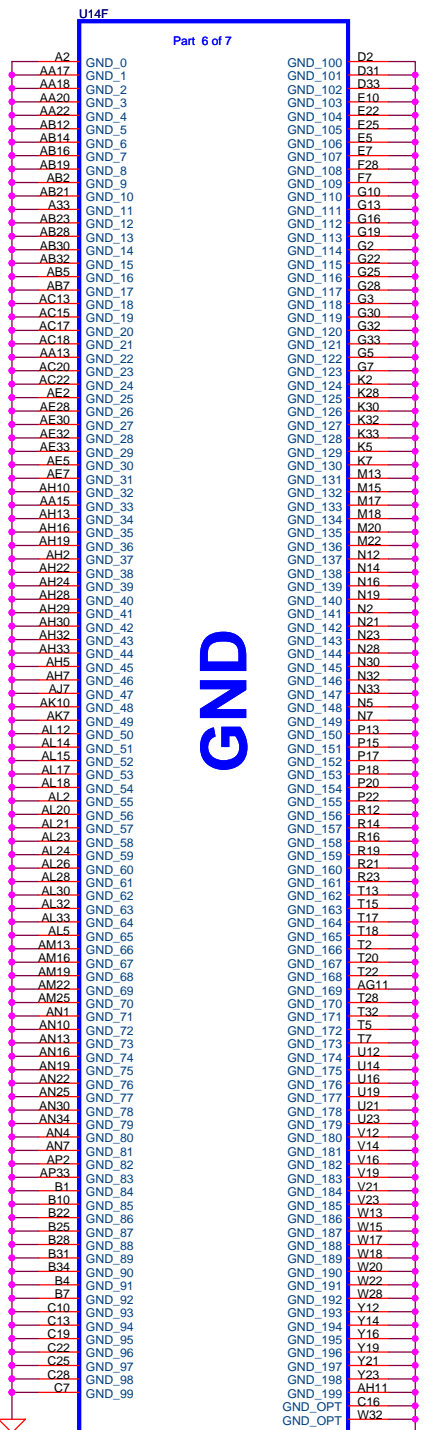


4 DIS@ 1 2 0.1U_0402_16V4Z

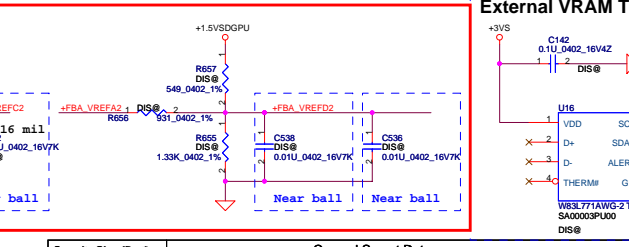
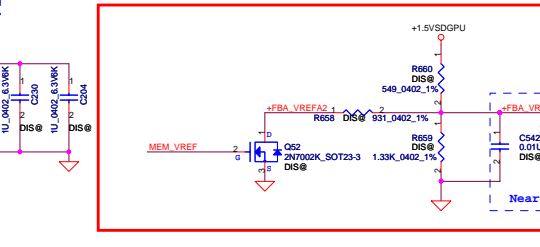
2 NV Remove IFPC_RSET,
D_RSET,IFPEF_RSET



| | | | | | | | |
|--|--------------------|-----------------|------------|---------------------------------|----------------------------------|----|----|
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| | | | | <i>4019J1</i> | | | |
| Date: Thursday, June 14, 2012 | | | | Sheet | 25 | of | 56 |



| | | | | | |
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| | | | | Date: Thursday, June 14, 2012 | Sheet 26 of 56 |



| | DATA Bus | |
|---------|----------|---------|
| Address | 0..31 | 32..63 |
| CMD0 | CS# | |
| CMD1 | A3_BA3 | |
| CMD2 | A2_BA0 | |
| CMD3 | A4_BA2 | |
| CMD4 | A5_BA1 | |
| CMD5 | WE# | |
| CMD6 | A7_A8 | |
| CMD7 | A6_A11 | |
| CMD8 | ABI# | |
| CMD9 | A12_RFU | |
| CMD10 | A0_A10 | |
| CMD11 | A1_A9 | |
| CMD12 | RAS# | |
| CMD13 | RST# | |
| CMD14 | CKE# | |
| CMD15 | CAS# | |
| CMD16 | | CS# |
| CMD17 | | A3_BA3 |
| CMD18 | | A2_BA0 |
| CMD19 | | A4_BA2 |
| CMD20 | | A5_BA1 |
| CMD21 | | WE# |
| CMD22 | | A7_A8 |
| CMD23 | | A6_A11 |
| CMD24 | | ABI# |
| CMD25 | | A12_RFU |
| CMD26 | | A0_A10 |
| CMD27 | | A1_A9 |
| CMD28 | | RAS# |
| CMD29 | | RST# |
| CMD30 | | CKE# |
| CMD31 | | CAS# |

| VRAM BOM Config | | | | |
|-----------------|--------|--------|------|---|
| X76364B0L01: | 1G HYN | 128*16 | 2.5G | SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABOI) |

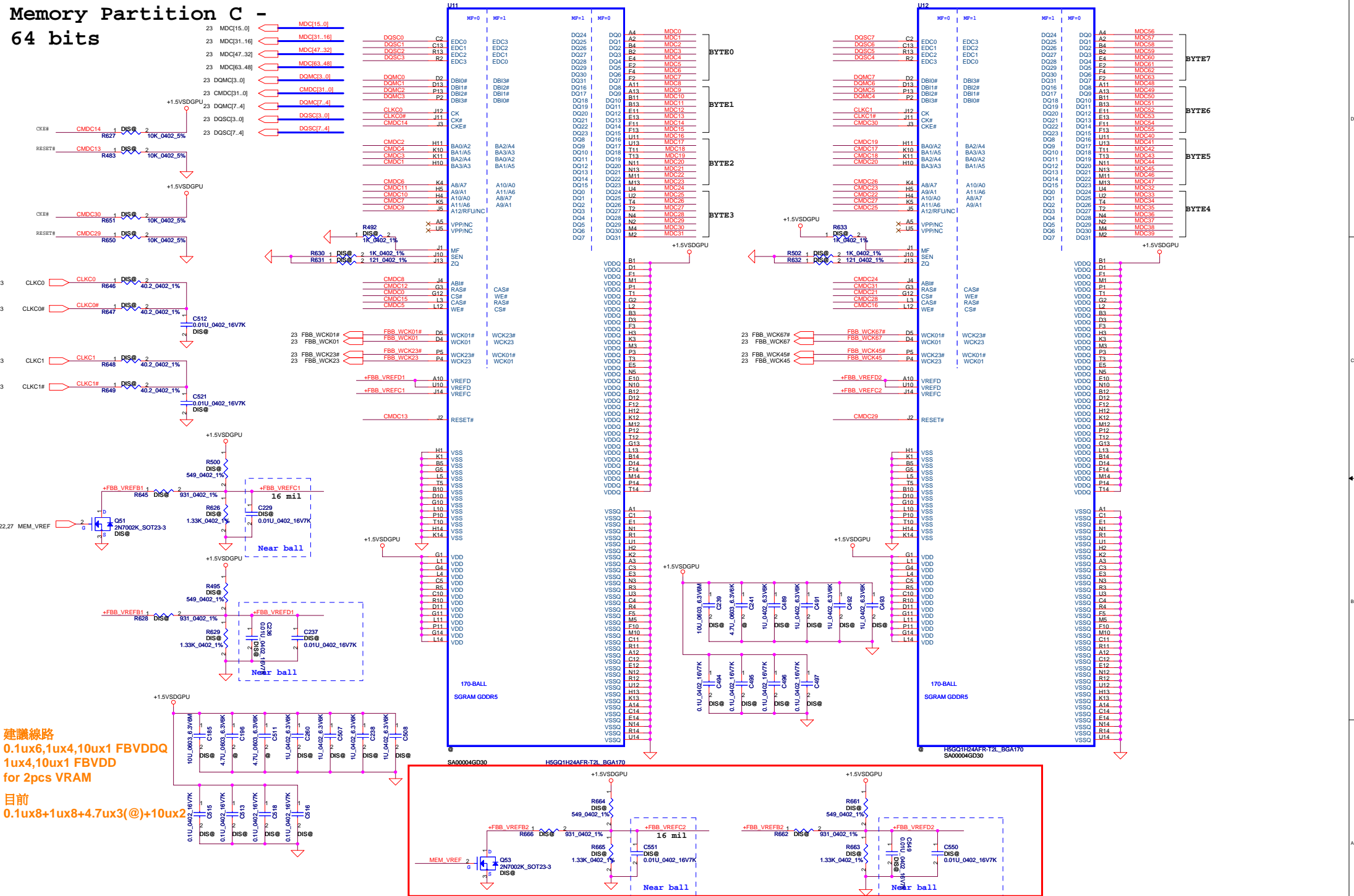
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|---|------------|--------------------|------------|--------------------------|------------------|
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| Issued Date | 2011/06/24 | Deciphered Date | 2012/06/02 | Title | |
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| | | | | Customer | 40191 |
| | | | | Date | 1993 Jun 14 2012 |
| | | | | Sheet | 27 of 56 |

Memory Partition C - 64 bits

建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

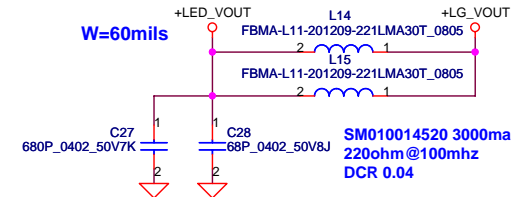
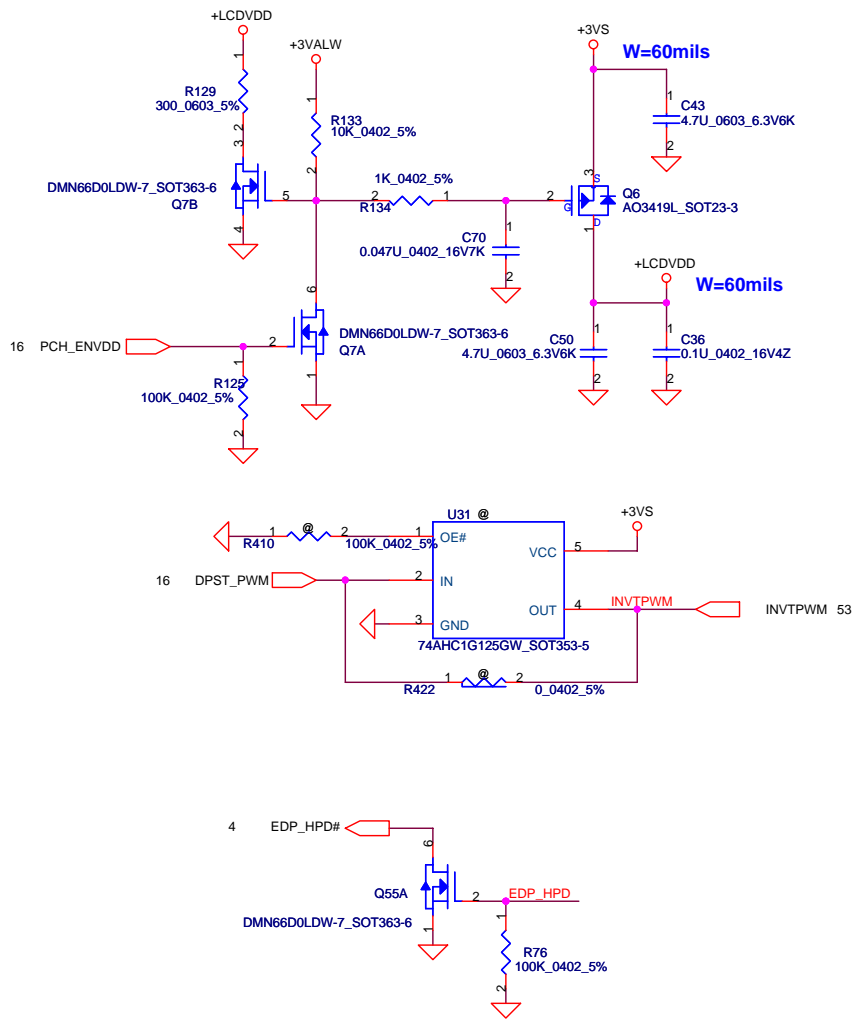
目前
0.1ux8+1ux8+4.7ux3(@)+10ux2

WWW.AliSaler.Com

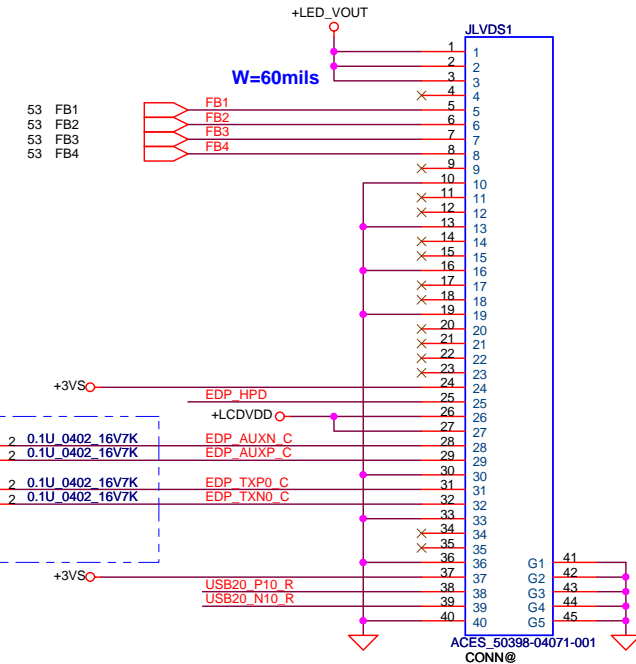


| | | | | | |
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| | | | | 4019J1 | |
| | | | | Date: Thursday, June 14, 2012 | Sheet 28 of 56 |

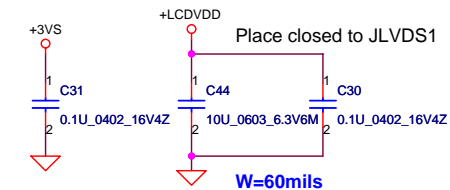
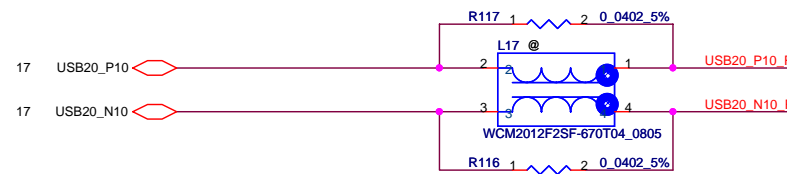
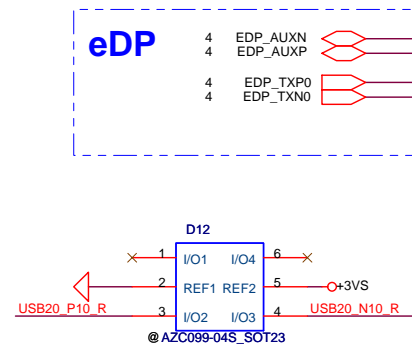
LCD POWER CIRCUIT



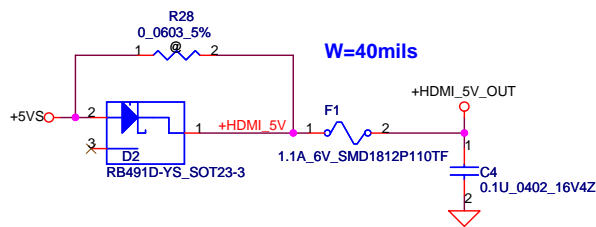
LCD/LED PANEL Conn.



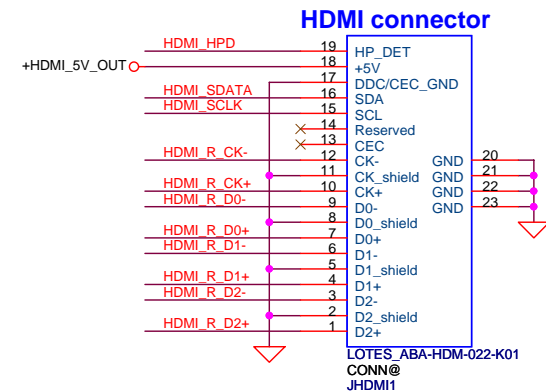
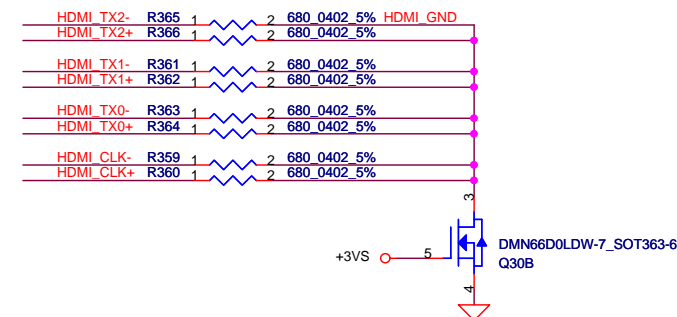
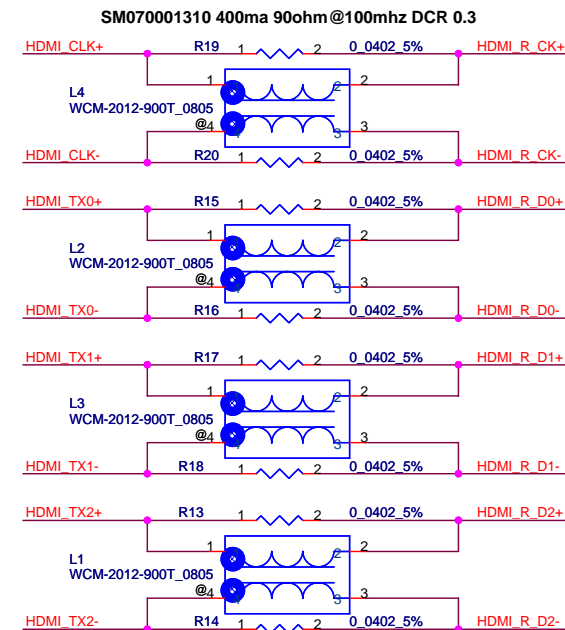
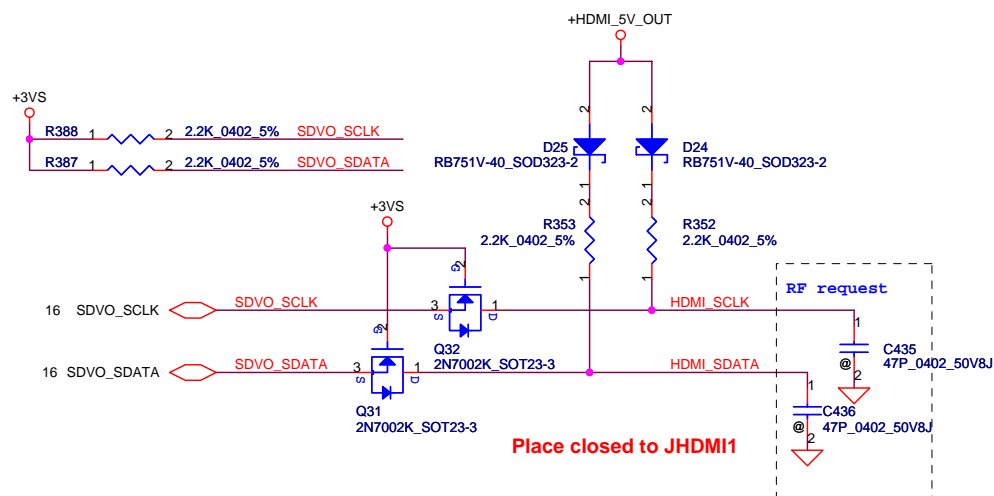
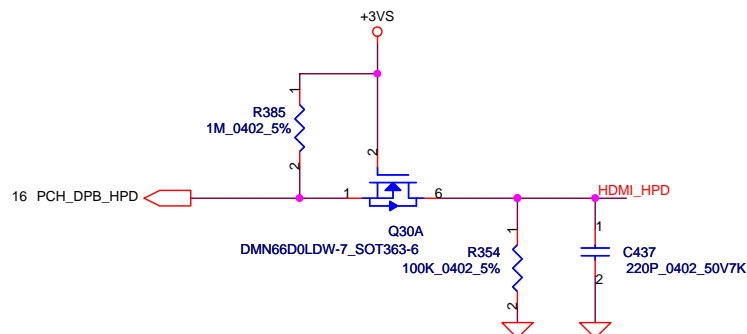
eDP



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| | | | | Date: Thursday, June 14, 2012 | Sheet 29 of 56 |

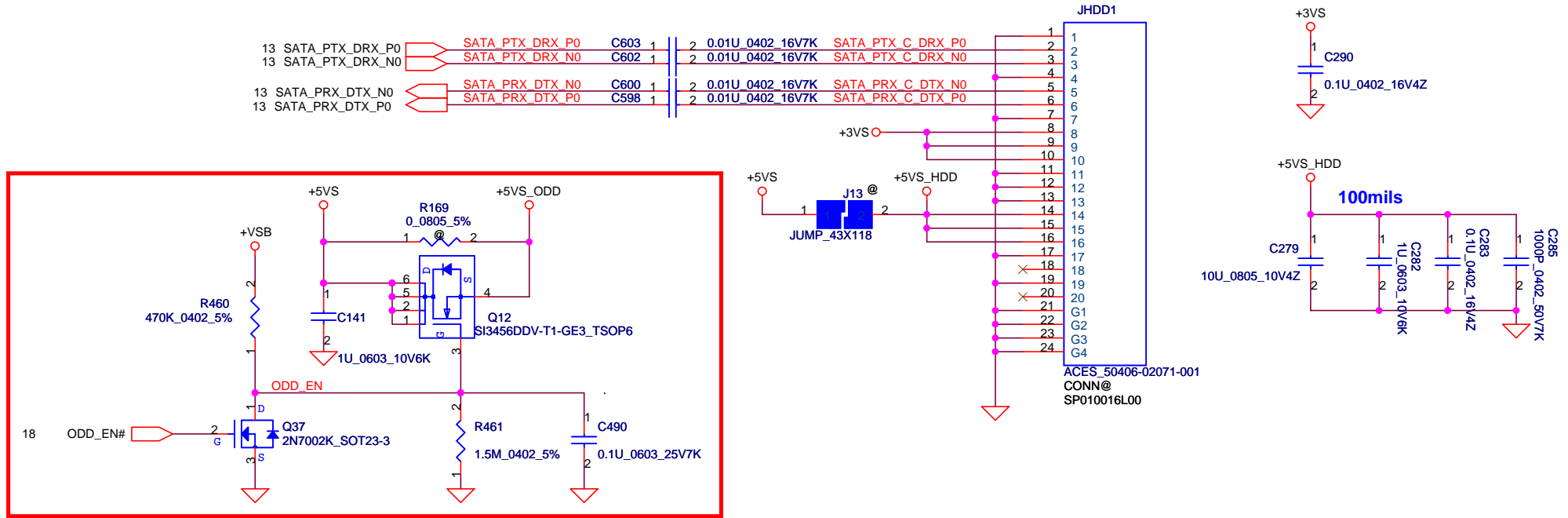


| | | | | | |
|---------------|-----|---|---|-----------------|-----------|
| 16 PCH_DPB_N0 | C7 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX2- |
| 16 PCH_DPB_P0 | C6 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX2+ |
| 16 PCH_DPB_N1 | C11 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX1- |
| 16 PCH_DPB_P1 | C10 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX1+ |
| 16 PCH_DPB_N2 | C9 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX0- |
| 16 PCH_DPB_P2 | C8 | 2 | 1 | 0.1U_0402_16V7K | HDMI TX0+ |
| 16 PCH_DPB_N3 | C13 | 2 | 1 | 0.1U_0402_16V7K | HDMI CLK- |
| 16 PCH_DPB_P3 | C12 | 2 | 1 | 0.1U_0402_16V7K | HDMI CLK+ |

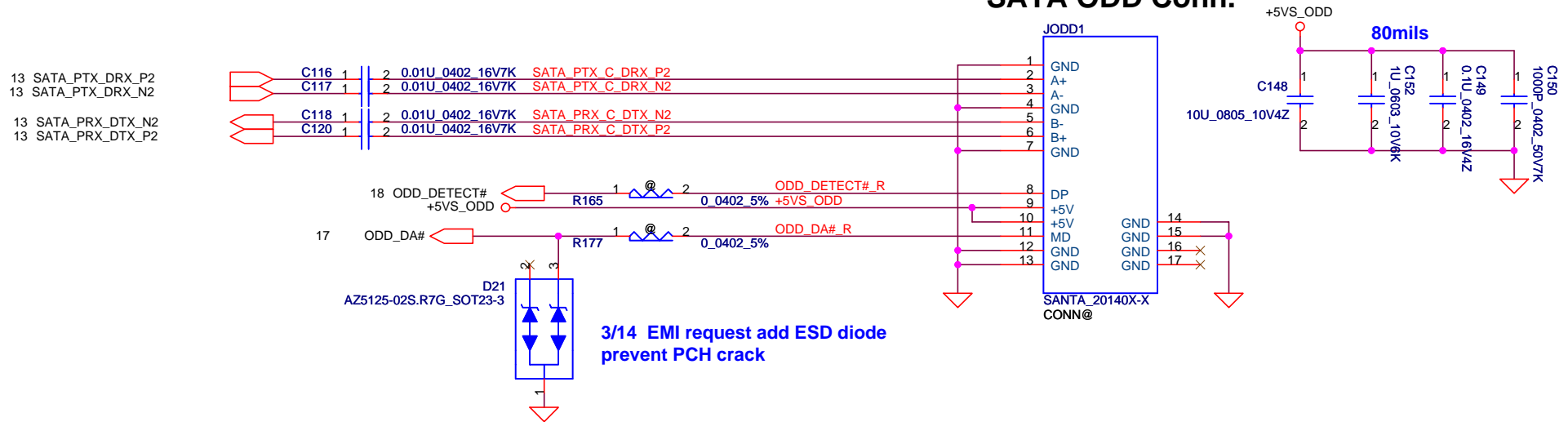


| | | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------|----------------|
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| | | | | Custom | 4019J1 | C |
| | | | | Date: | Thursday, June 14, 2012 | Sheet 30 of 56 |

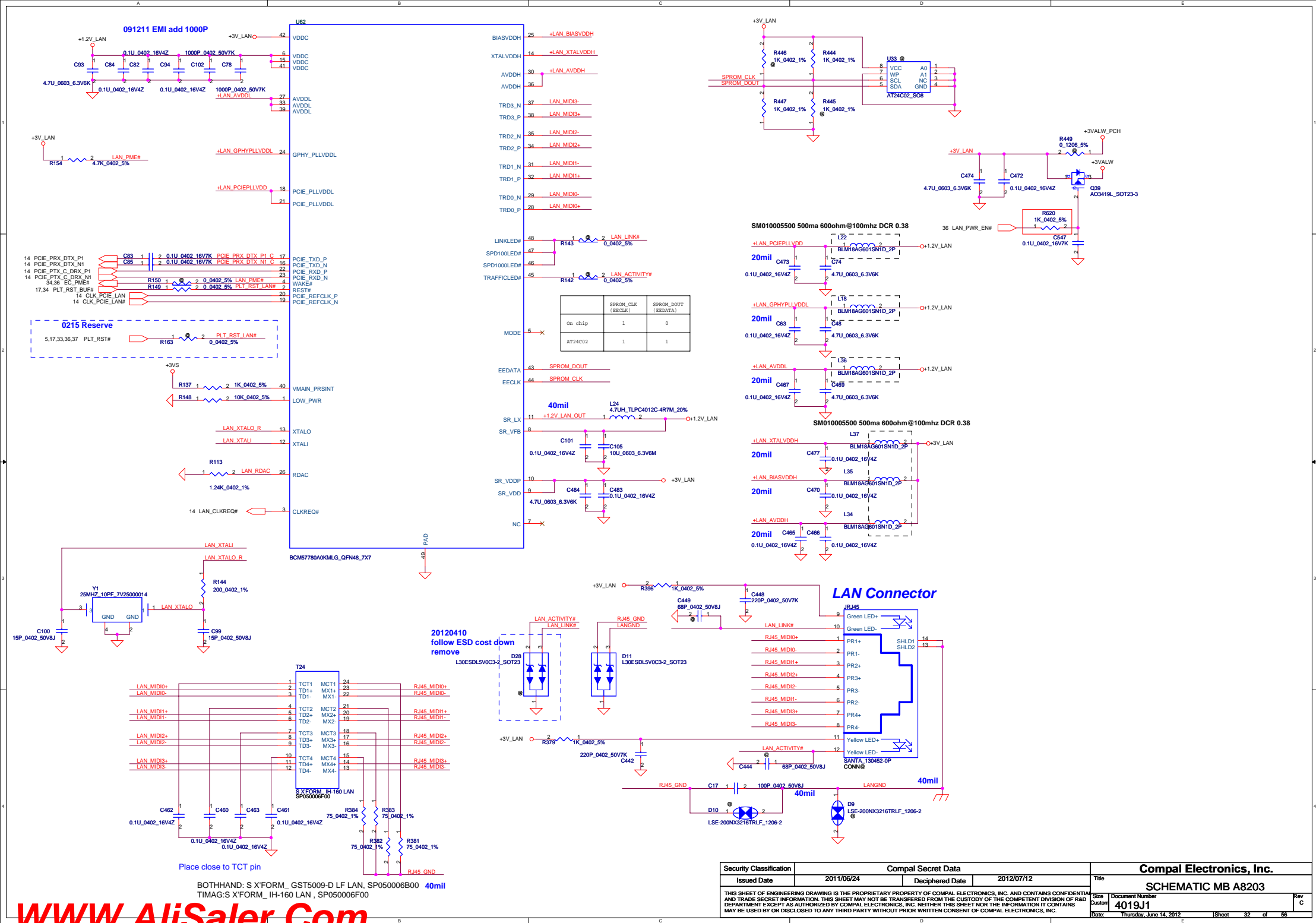
SATA HDD1 Conn.



SATA ODD Conn.

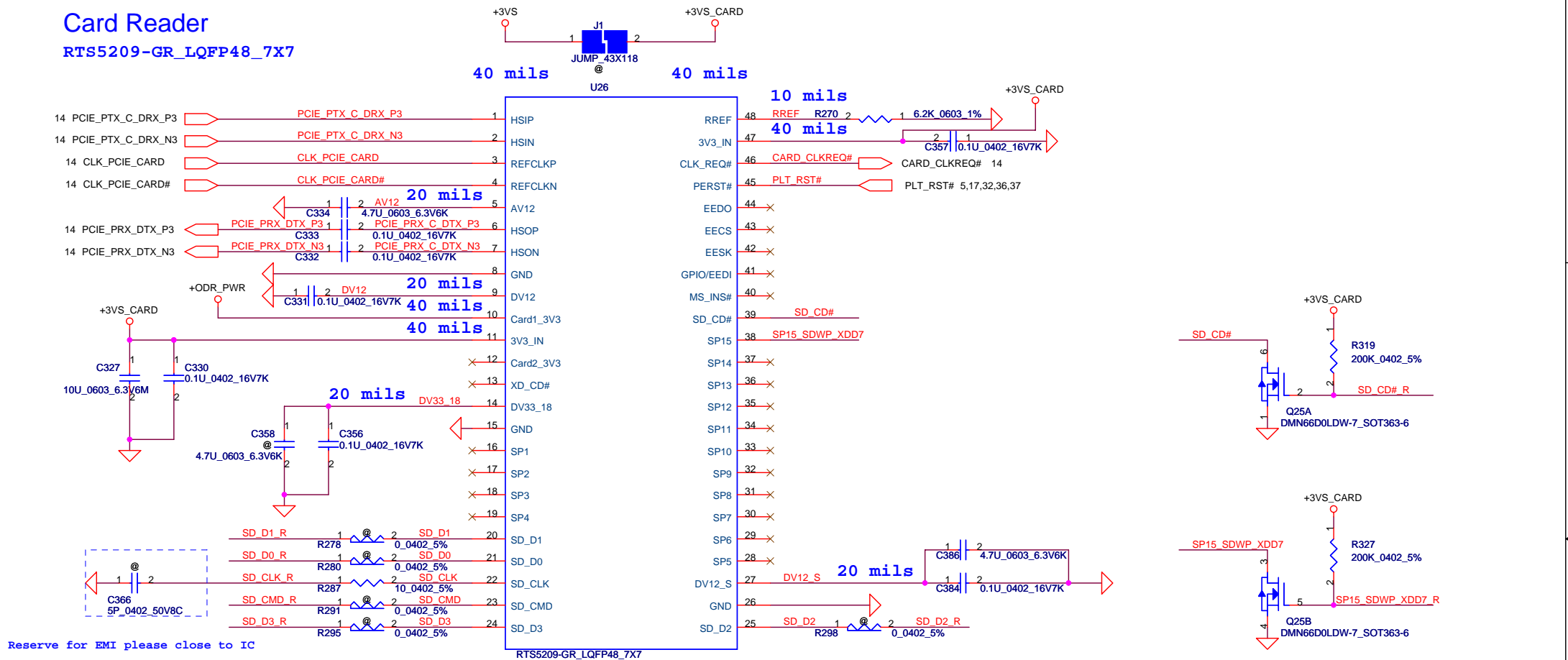


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| Date: Thursday, June 14, 2012 | | | | Sheet 31 of 56 |



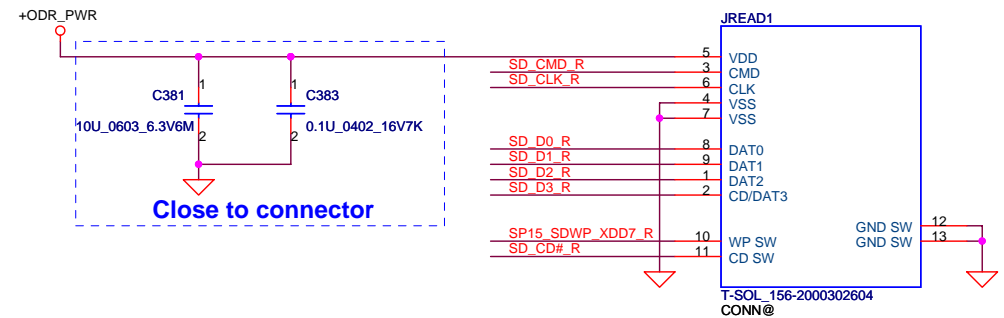
Card Reader

RTS5209-GR_LQFP48_7X7



Reserve for EMI please close to IC

| Pin No. | Name |
|---------|-----------------------|
| 1 | DAT2 |
| 2 | DAT3 |
| 3 | CMD |
| 4 | VSS |
| 5 | VDD |
| 6 | CLK |
| 7 | VSS |
| 8 | DAT0 |
| 9 | DAT1 |
| 10 | WP Pin (Normal close) |
| 11 | CD Pin (Normal close) |

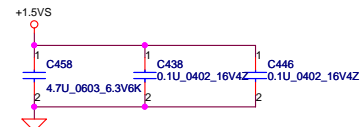
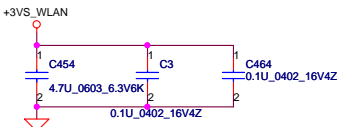
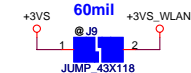
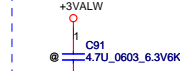


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|---|-------------------------|-----------------|------------|--------------------------|--------------------|
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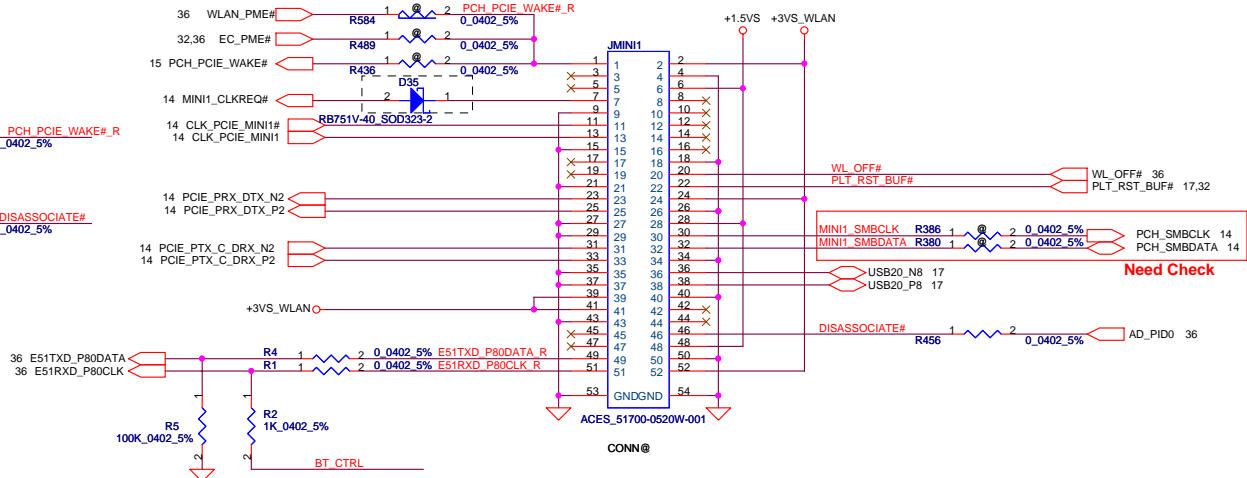
For Wireless LAN

| | BT on module Enable | BT on module Disable |
|---------|------------------------|-------------------------|
| BT_CTRL | H | L |
| BT_ON# | L | H |

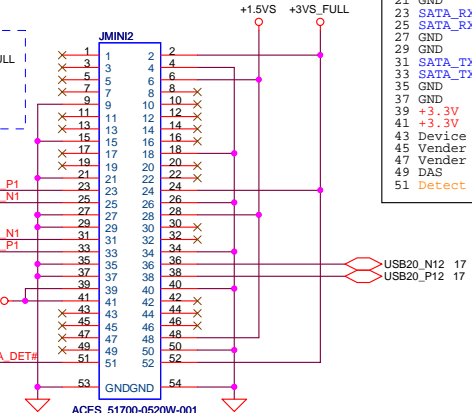
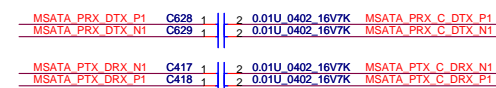
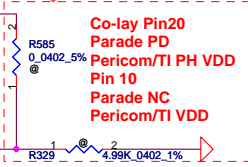
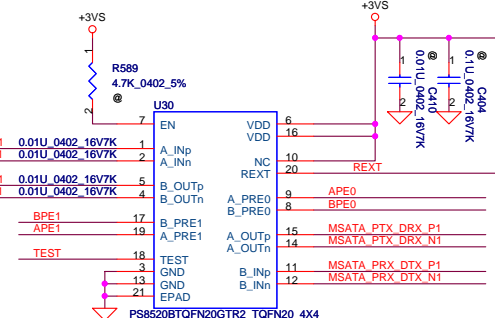
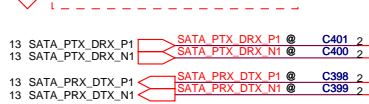
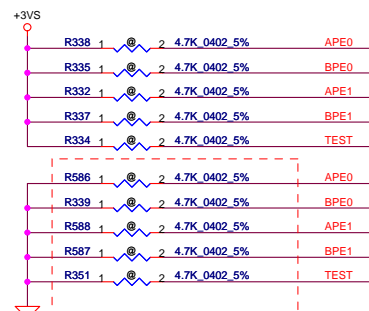
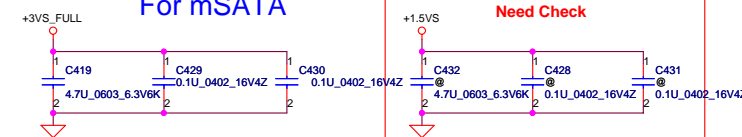
36



Mini Card Power Rating



For mSATA

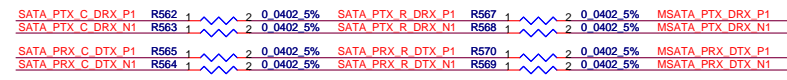


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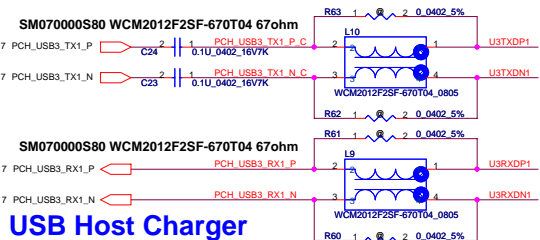
MSATA pin define
1 Reserved 2 +3.3V
3 Reserved 4 GND
5 Reserved 6 +1.5V
7 Reserved 8 Reserved
9 GND 10 Reserved
11 Reserved 12 Reserved
13 Reserved 14 Reserved
15 GND 16 Reserved
17 Reserved 18 GND
19 Reserved 20 Reserved
21 GND 22 Reserved
23 SATA_RX_P 24 +3.3V
25 SATA_RX_N 26 GND
27 GND 28 +1.5V
29 GND 30 SMB_CLK
31 SATA_TX_N 32 SMB_DATA
33 SATA_TX_P 34 GND
35 GND 36 Reserved
37 GND 38 Reserved
39 +3.3V 40 GND
41 +3.3V 42 Reserved
43 Device Type 44 Reserved
45 Vendor define 46 Vendor define
47 Vendor define 48 +1.5V
49 DAS 50 GND
51 Detect 52 +3.3V

```

MSATA SATA3.0 Repeater

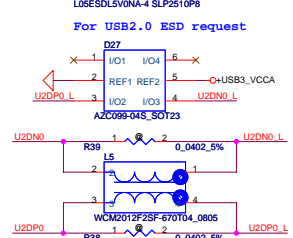
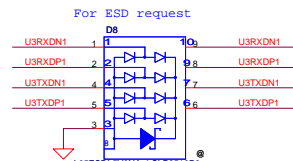
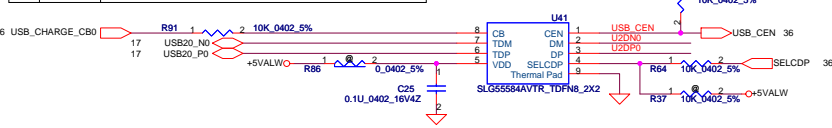


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| | | | | Custm | 4019J1 | C |
| | | | | Date: | Thursday, June 14, 2012 | Sheet 34 of 56 |

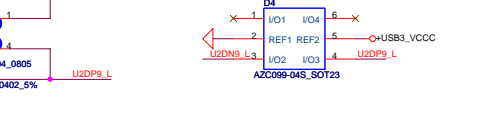
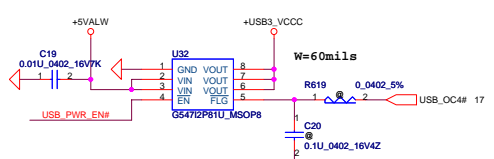
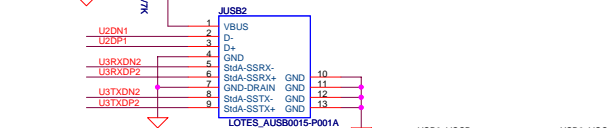
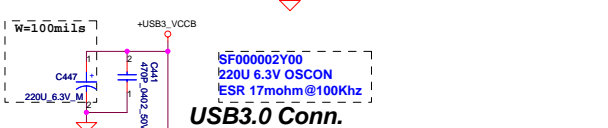
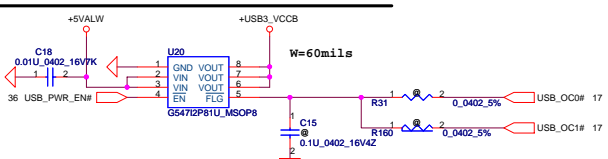
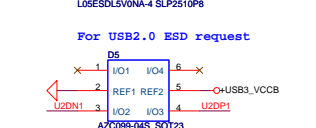
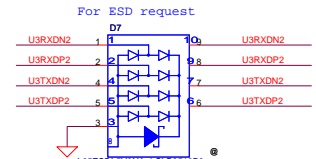
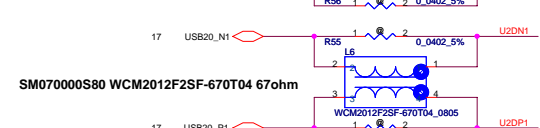
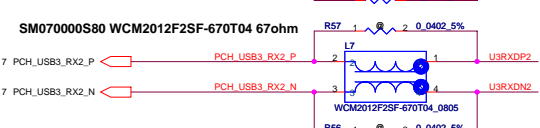
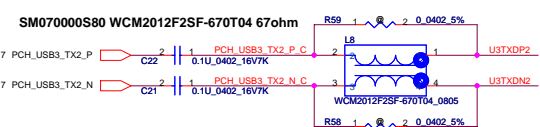
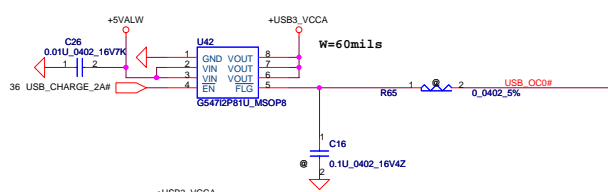


USB Host Charger

| CB | SELCDP | |
|----|--------|--|
| 0 | X | DCP(Dedicated Charging Port) autotetect with mouse/keyboard wakeup |
| 1 | 0 | S0 charging with SDP(Standard Downstream Port) only |
| 1 | 1 | S0 charging with CDP(Charging Downstream Port) or SDP only |

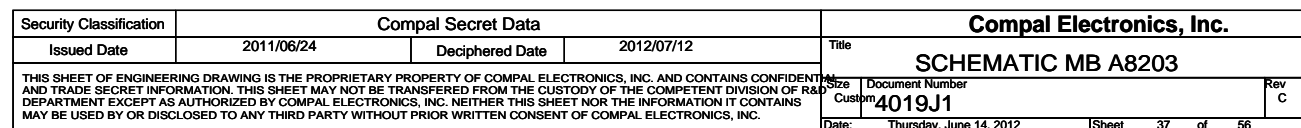


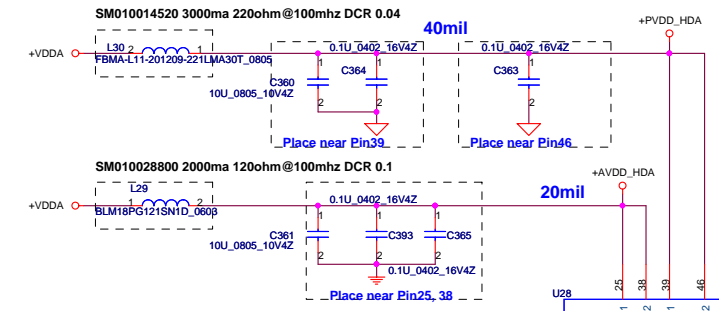
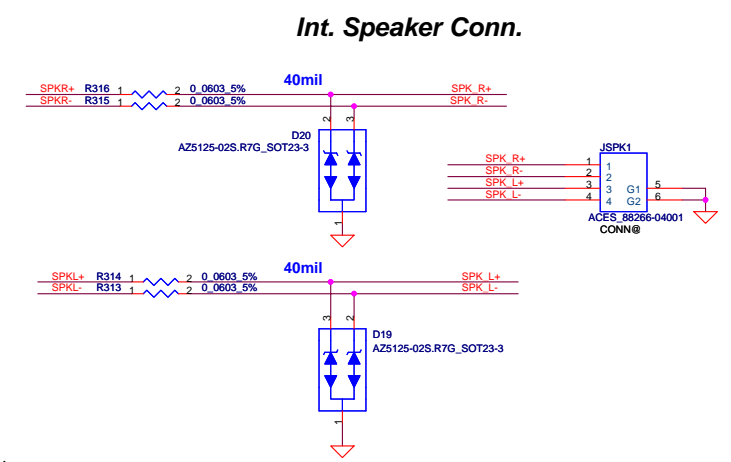
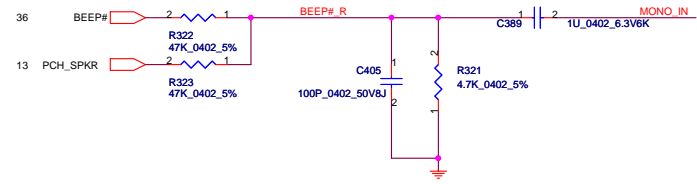
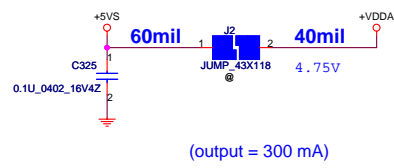
SM070000S80 WCM2012F2SF-670T04 67ohm



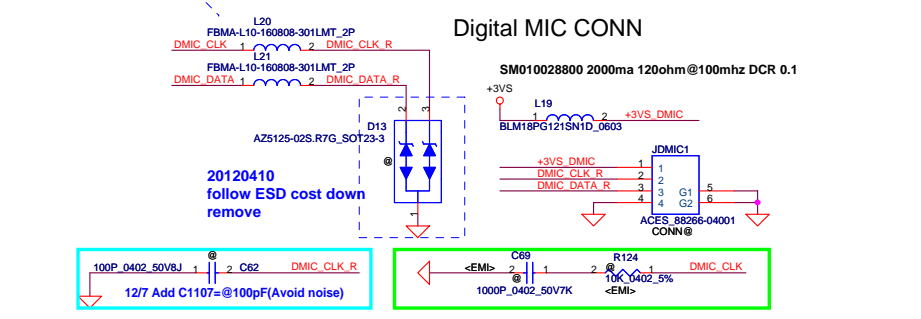
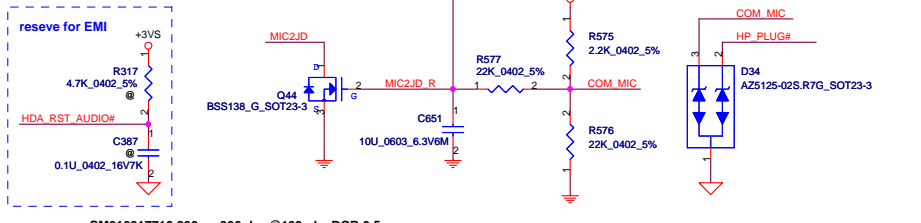
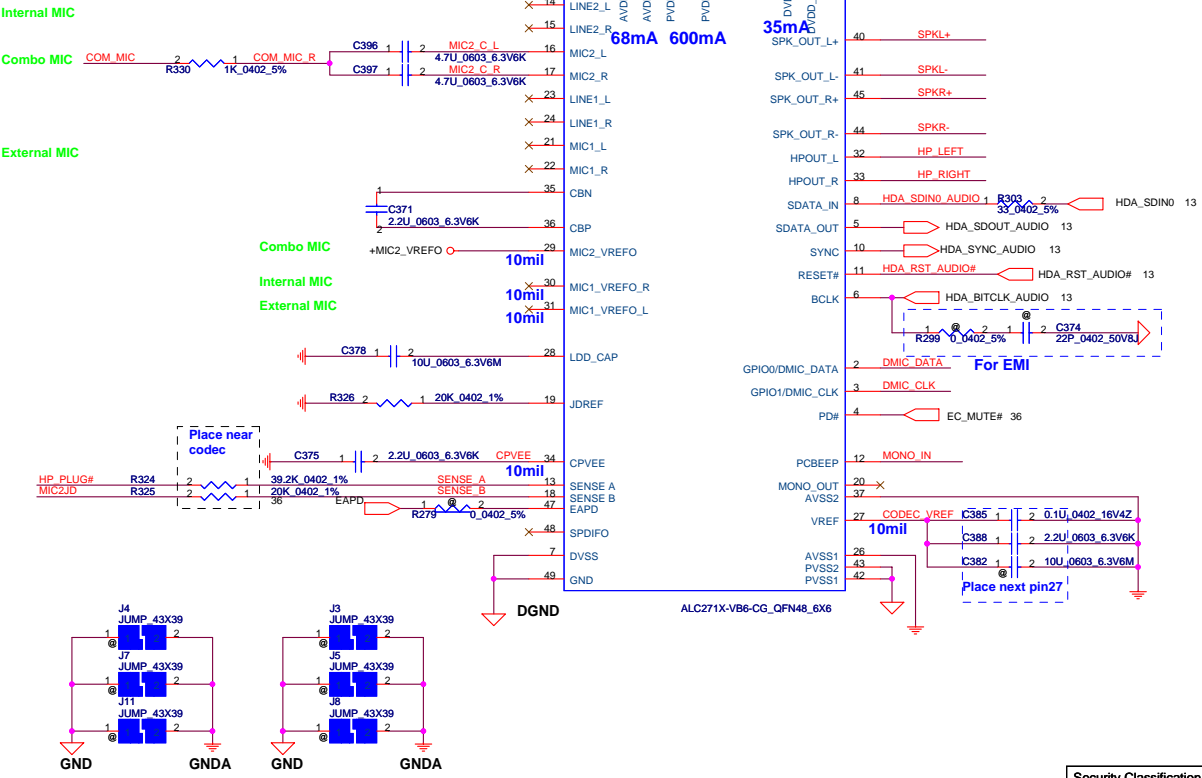
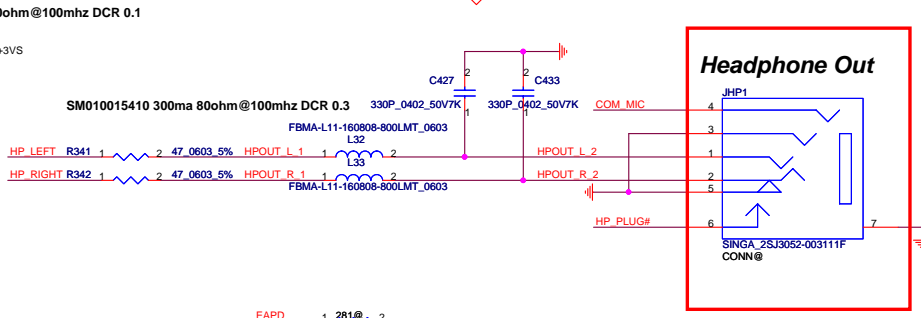
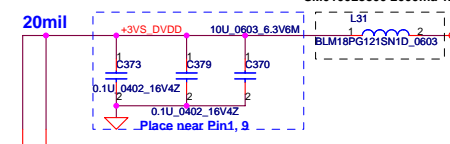
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| Date: Thursday, June 14, 2012 | | Sheet | 35 of 56 |



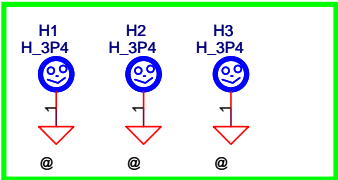
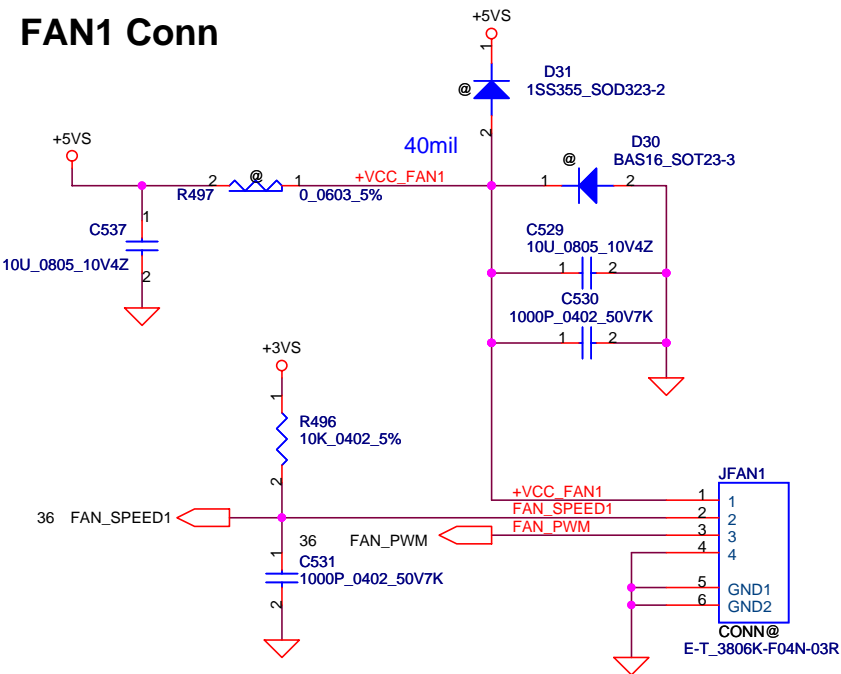




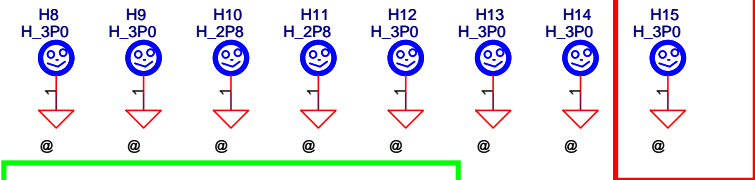
HD Audio Codec



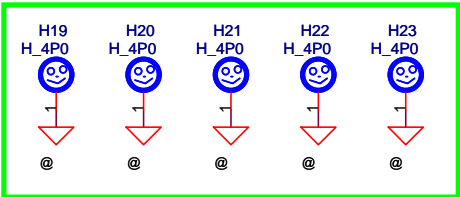
FAN1 Conn



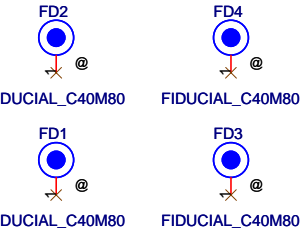
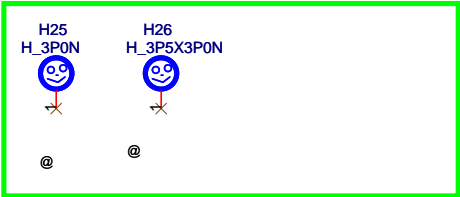
WLAN+MSATA Stand off



CPU,VGA support plate

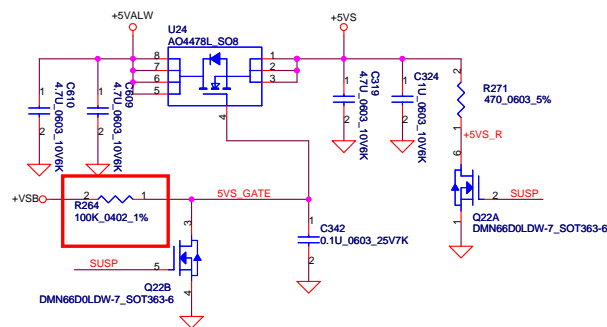


locate MB

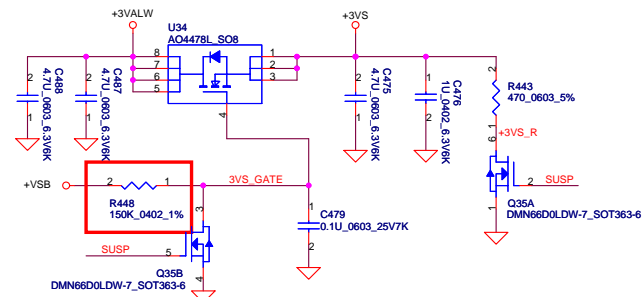


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| Date: | | Thursday, June 14, 2012 | | Sheet | 39 | of 56 |

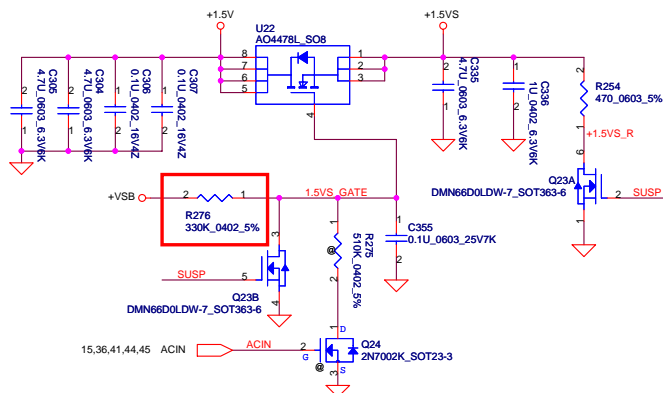
+5VALW TO +5VS



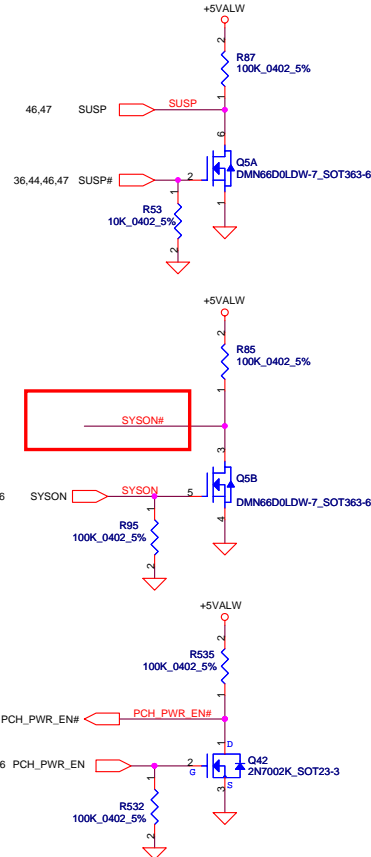
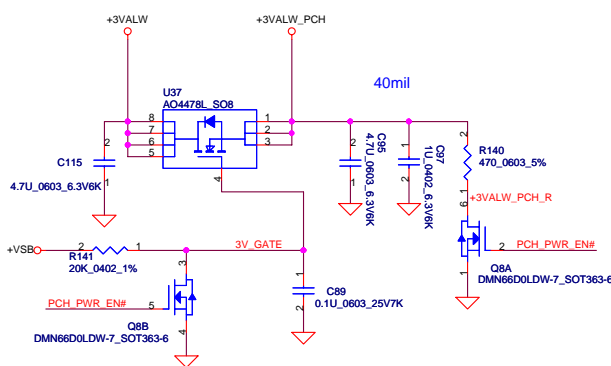
+3VALW TO +3VS



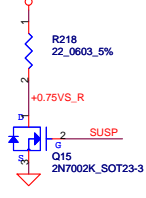
+1.5V to +1.5VS



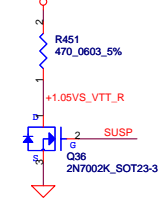
+3VALW TO +3VALW (PCH AUX Power) Short J5 for PCH VCCSUS3.3



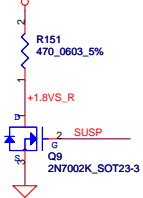
+0.75VS



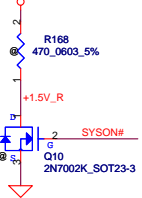
+1.05VS_VTT



+1.8VS

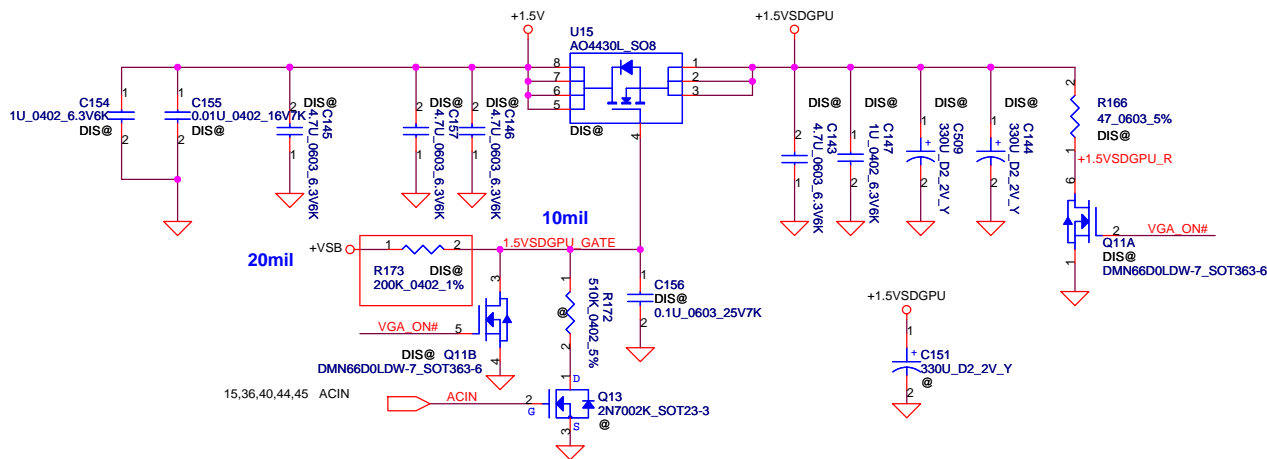


+1.5V

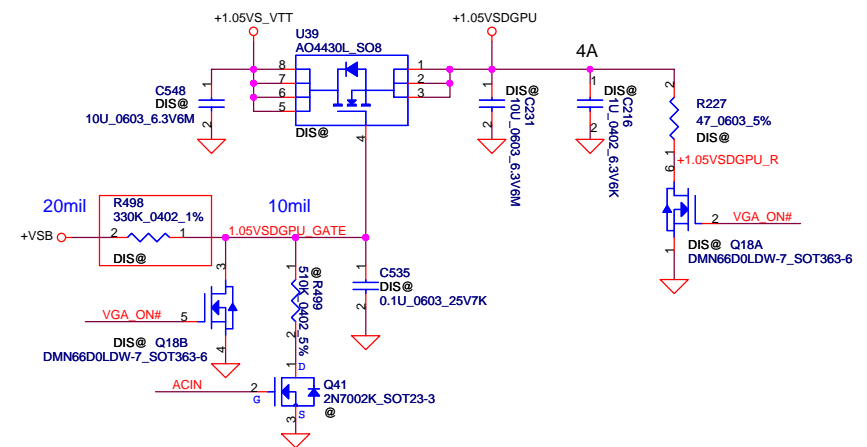


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| | | | | Thursday, June 14, 2012 |
| | | | | Sheet 40 of 56 |

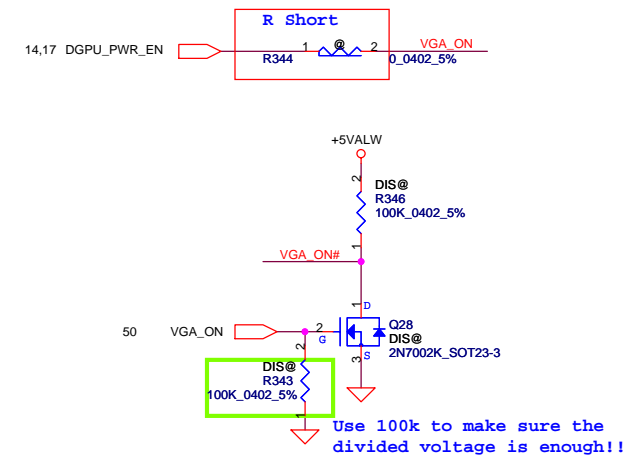
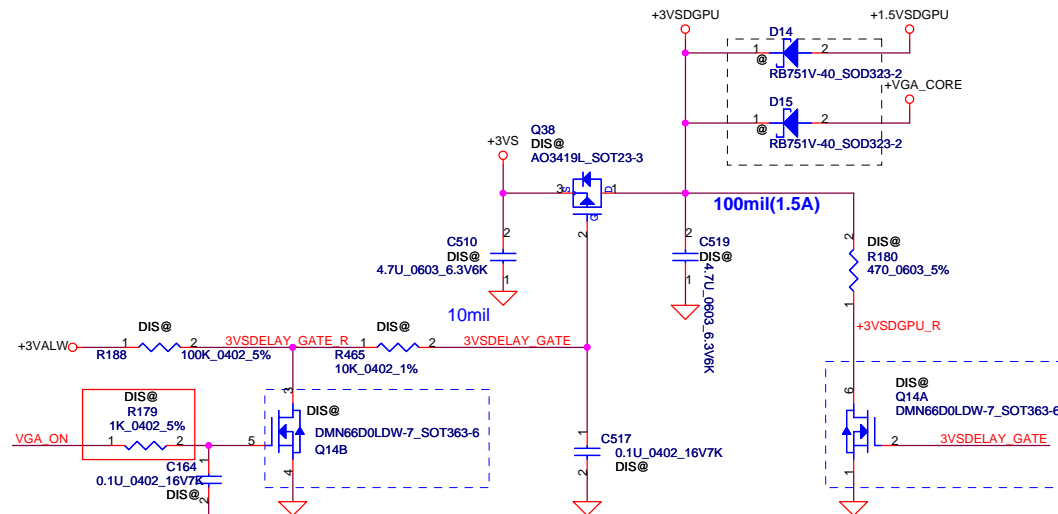
+1.5VSDGPUH to +1.5VSDGPU for GPU



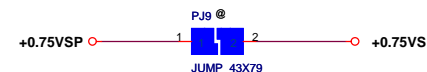
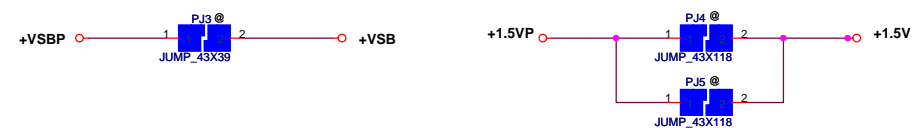
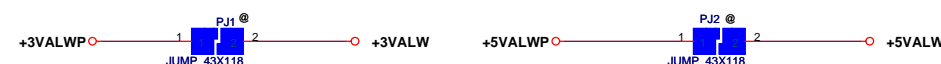
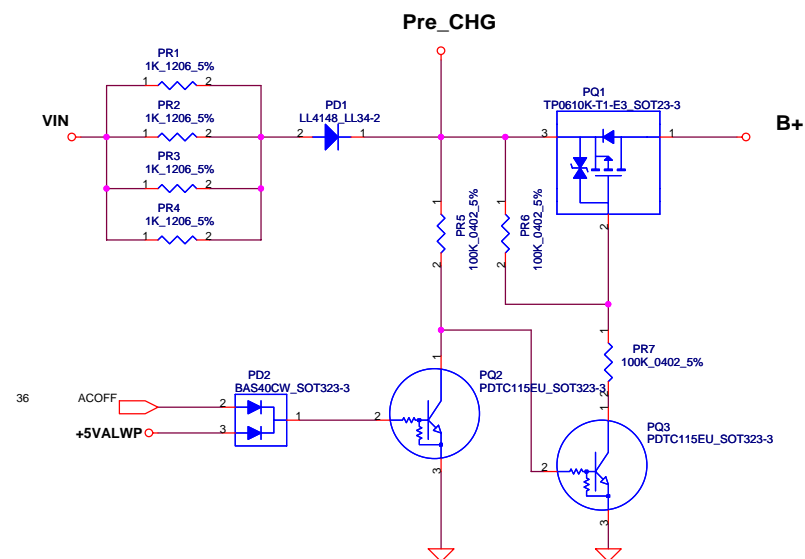
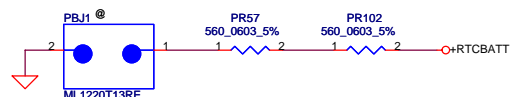
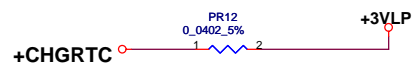
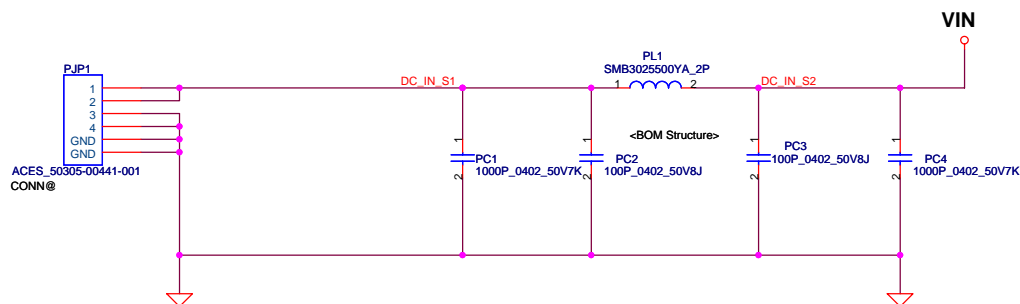
+1.05V_{S_VTT} to +1.05V_{SDGPU} for GPU



+3VS to +3VSDGPU for GPU

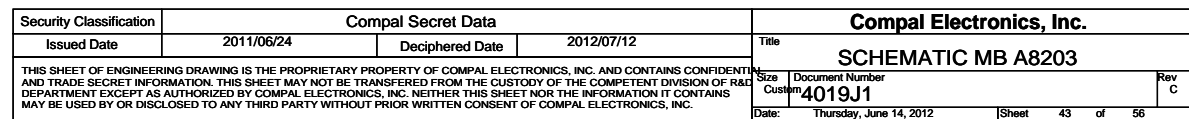


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| | | | | Customer Document Number | |
| | | | | Date: Thursday, June 14, 2012 | Sheet 41 of 56 |

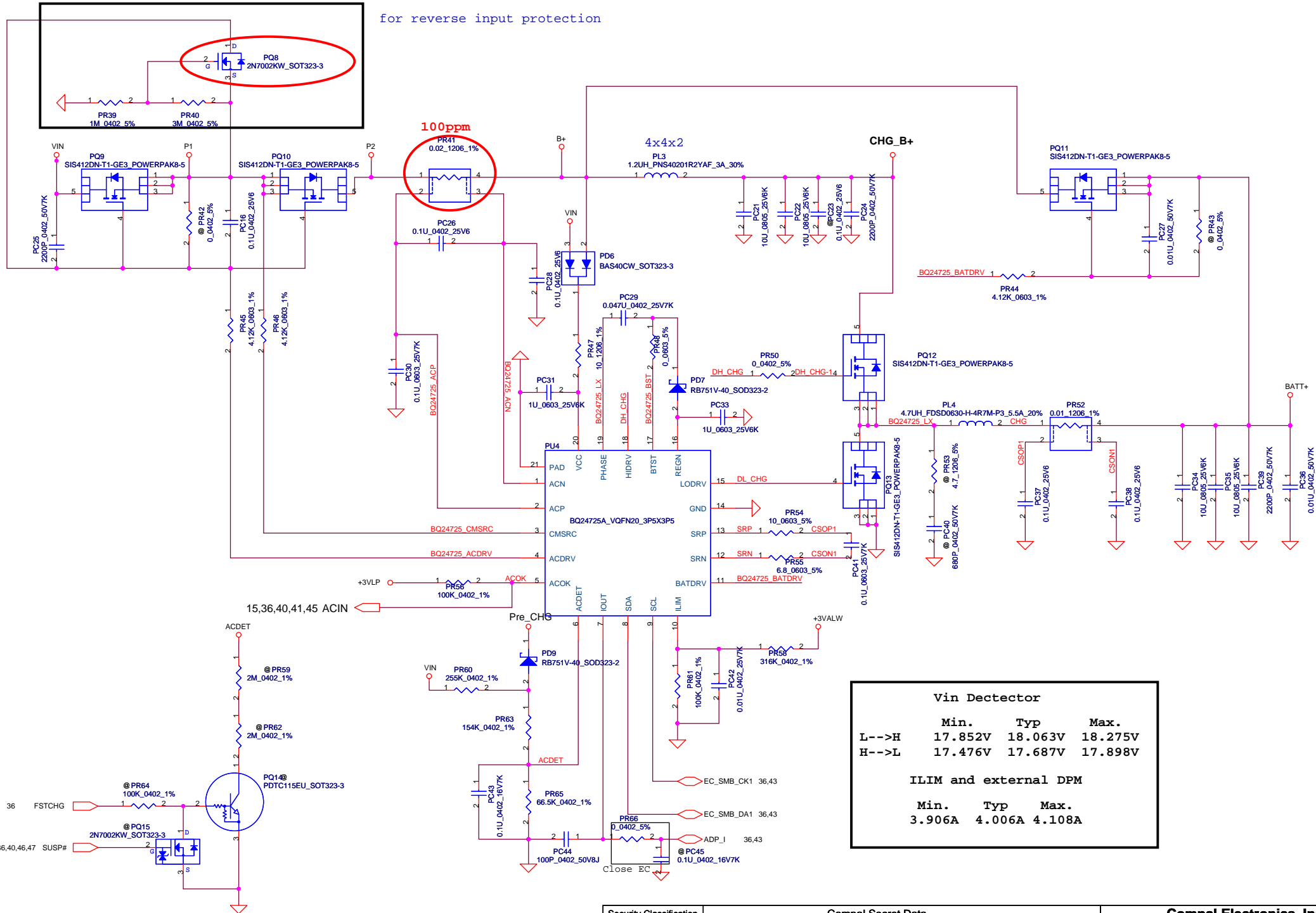


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| Document Number | | | | Rev C |
| 4019J1 | | | | |
| Date: Thursday, June 14, 2012 | | | | Sheet 42 of 56 |

ACES_50290-0100N

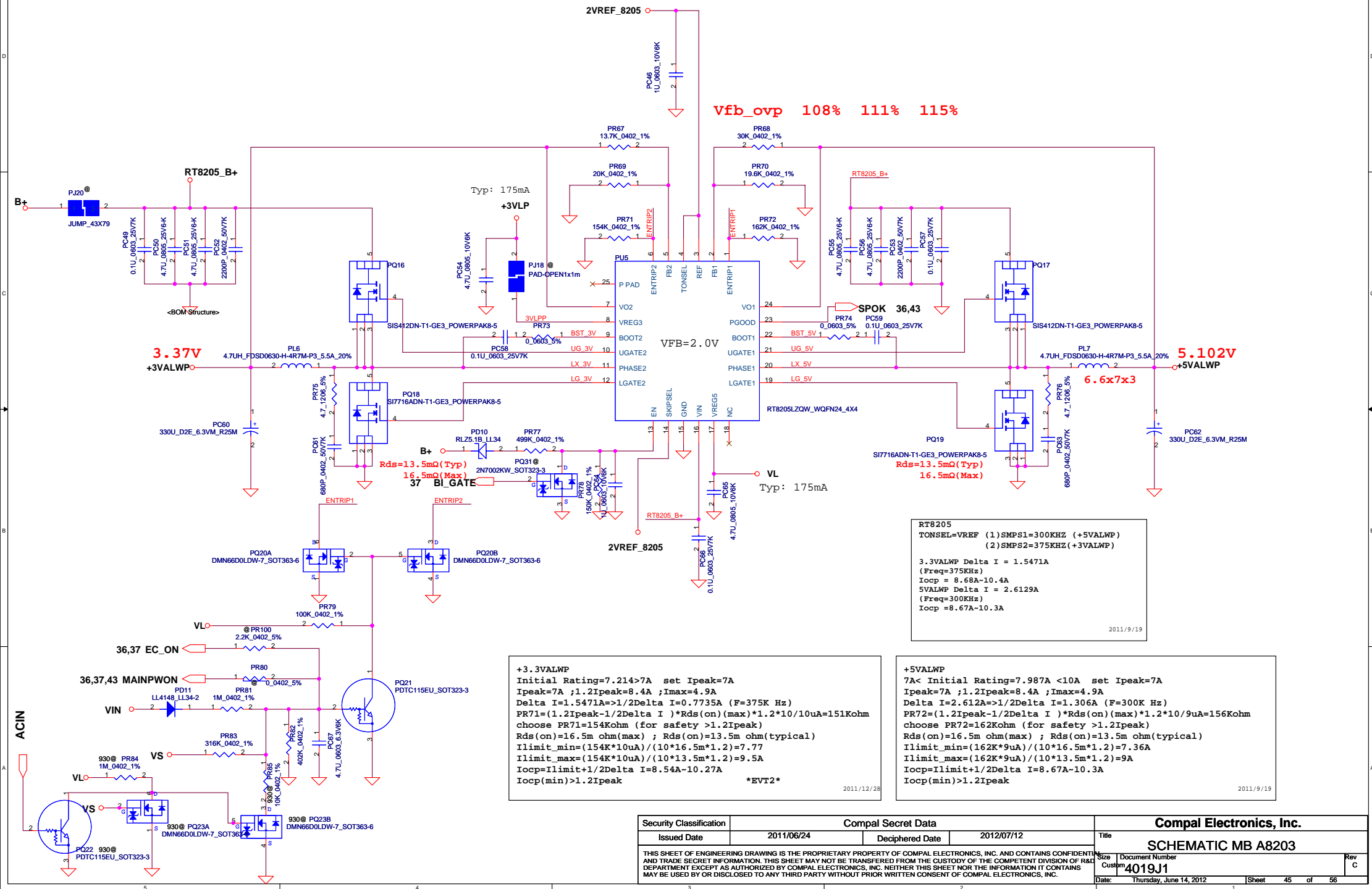


for reverse input protection



| | | | | | |
|---|-----------------|--------------------|-------------------------|--------------------------|--------------------|
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| Size | Document Number | Sheet | 44 | of | 56 |
| Custom | 4019J1 | Date: | Thursday, June 14, 2012 | Sheet | 44 |

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

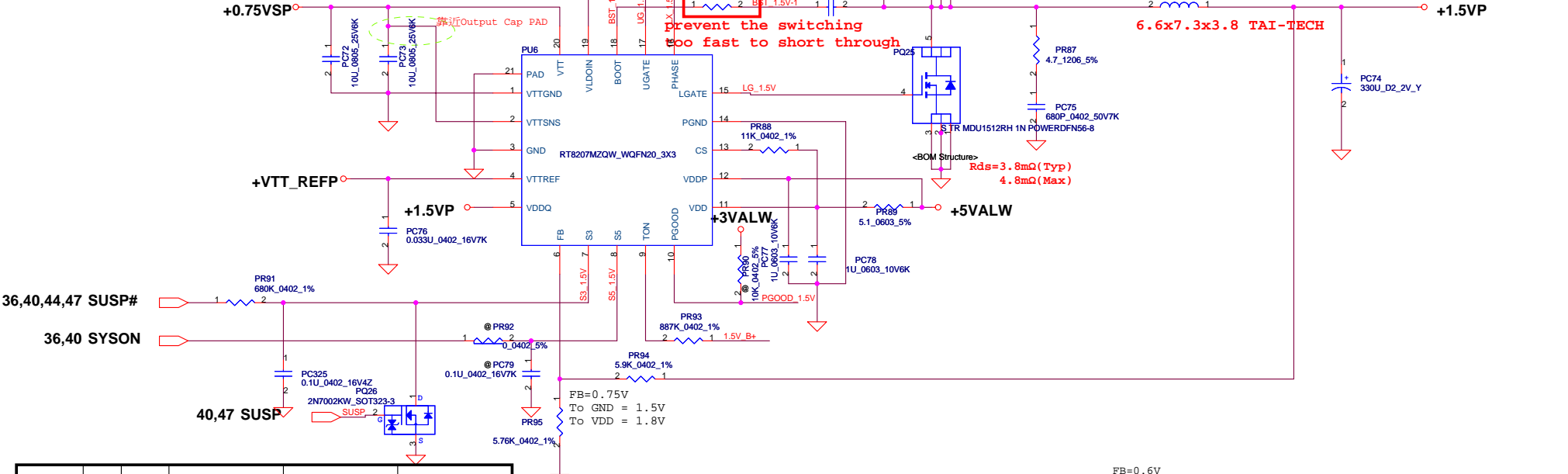


```

+1.5VP
Ipeak = max{ 07*Ibudget, 1st +2nd max loading}
Ipeak = max{ 20.85*0.7 , 5+8.2 }
Ipeak=14.59A ; 1.2Ipeak=17.51A ;Imax=10.21A
1/2Delta I=1.535A (F=300K Hz)
PR88=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=10.7Kohm
choose PR88=11Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(11K*9uA)/(4.8m*1.2)=17.2A
Ilimit_max=(11K*9uA)/(3.8m*1.2)=21.7A
Iocp=Ilimit+1/2Delta I=18.7A~23.2A
Iocp(min)>1.2Ipeak
  
```

2011/9/19

OVP=10% 15% 20%



36,40,44,47 SUSP#

36,40 SYSON

40,47 SUSP

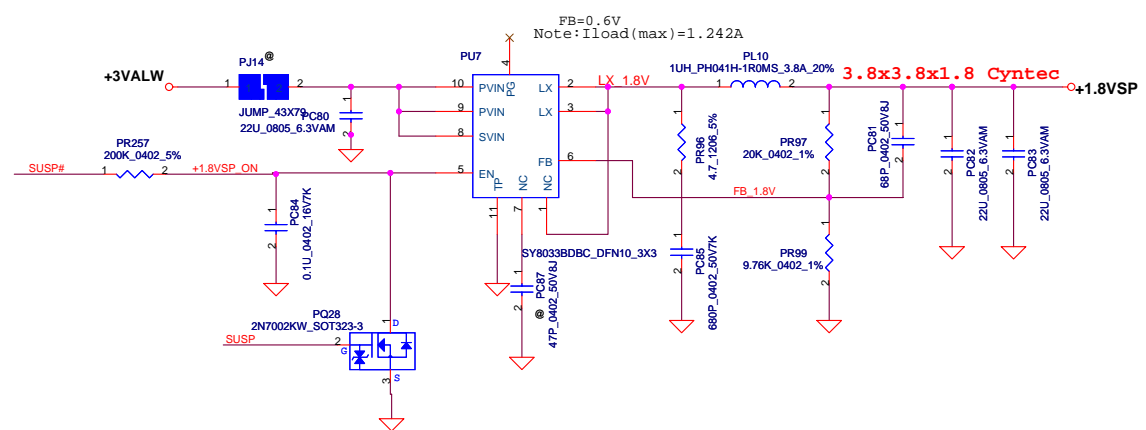
| STATE | S3 | S5 | 1.5VP | VTT_REFP | 0.75VSP |
|-------|----|----|-----------------|-----------------|-----------------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off (Discharge) | Off (Discharge) | Off (Discharge) |

Note: S3 - sleep ; S5 - power off

UMA

```

+1.5VP
Ipeak = max{ 07*Ibudget, 1st +2nd max loading}
Ipeak = max{ 15.05*0.7 , 5+8.2 }
Ipeak=13.2A ; 1.2Ipeak=15.84A ;Imax=9.24A
1/2Delta I=1.535A (F=300K Hz)
PR88=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=9.16Kohm
choose PR88=9.53Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(11K*9uA)/(4.8m*1.2)=14.9A
Ilimit_max=(11K*9uA)/(3.8m*1.2)=18.8A
Iocp=Ilimit+1/2Delta I=16.4A~20.3A
Iocp(min)>1.2Ipeak
  
```



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|---|------------|--------------------|------------|-----------------|-------------------------|
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WWW.AliSaler.Com

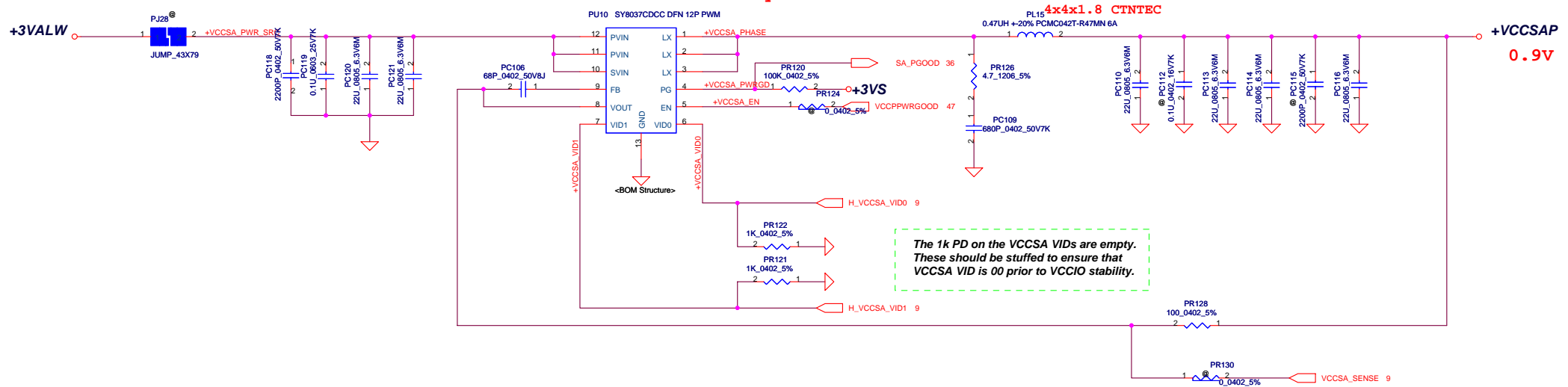
Note: Use VCCSA_SEL to switch High & Low level for VID[1]

| VID [0] | VID[1] | VCCSA Vout |
|---------|--------|------------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.85V |
| 1 | 0 | 0.775V |
| 1 | 1 | 0.75V |

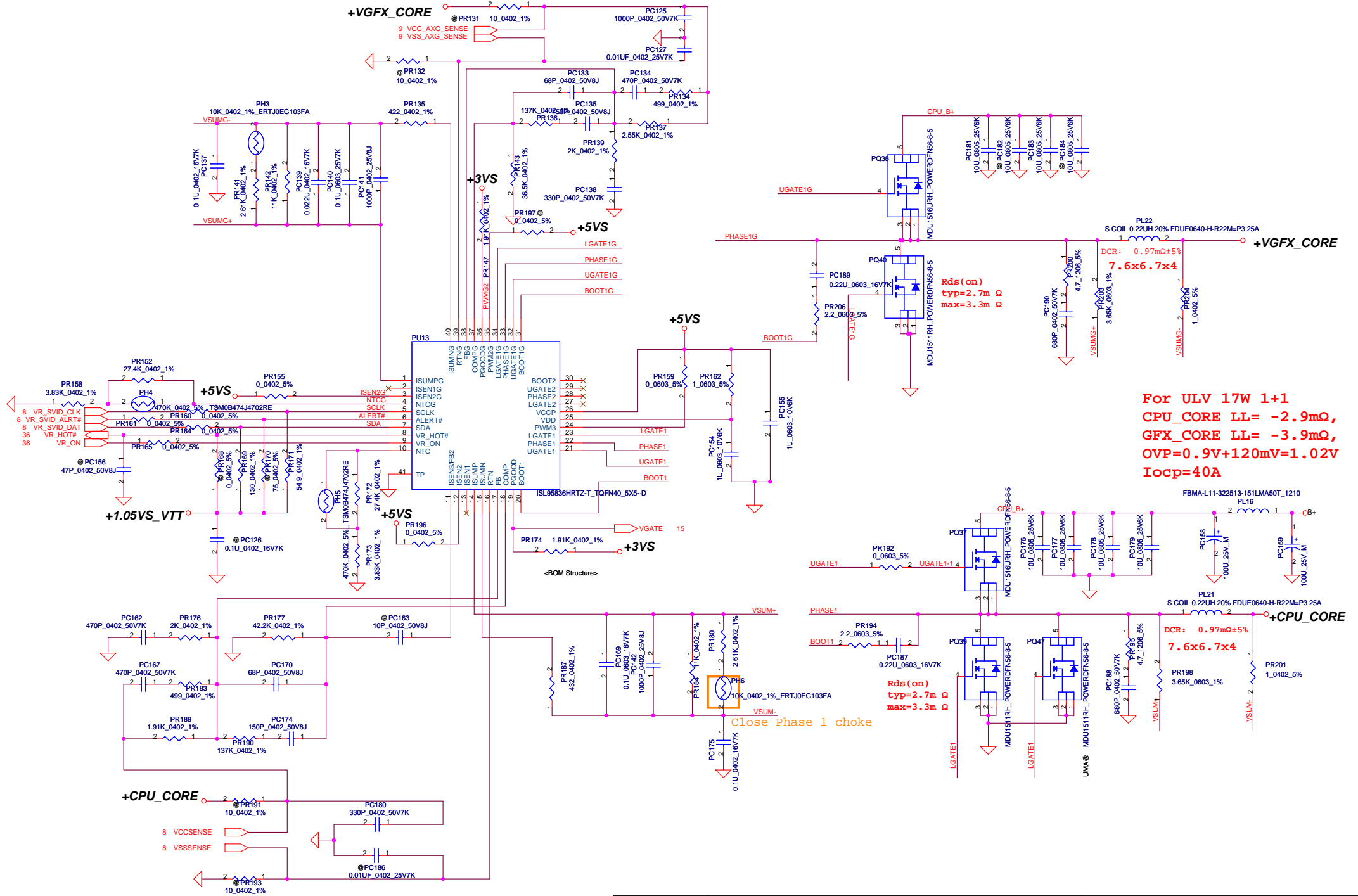
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

PU10 Has not Link 8037C yet

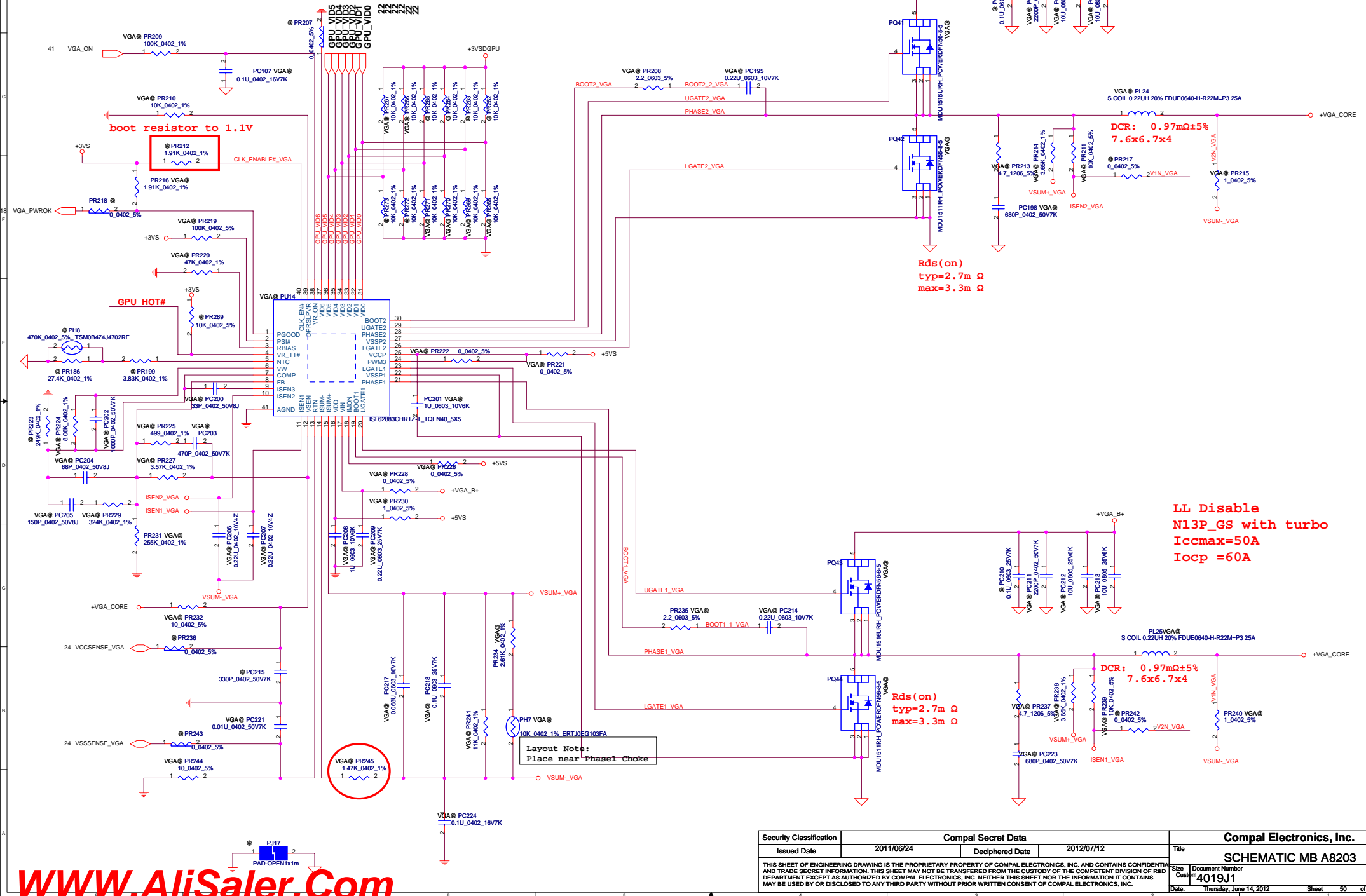


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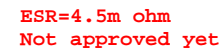
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| VGA Chipset | Default Voltage | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
|-------------|-----------------|------|------|------|------|------|------|------|
| N13P GS | 0.9V | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

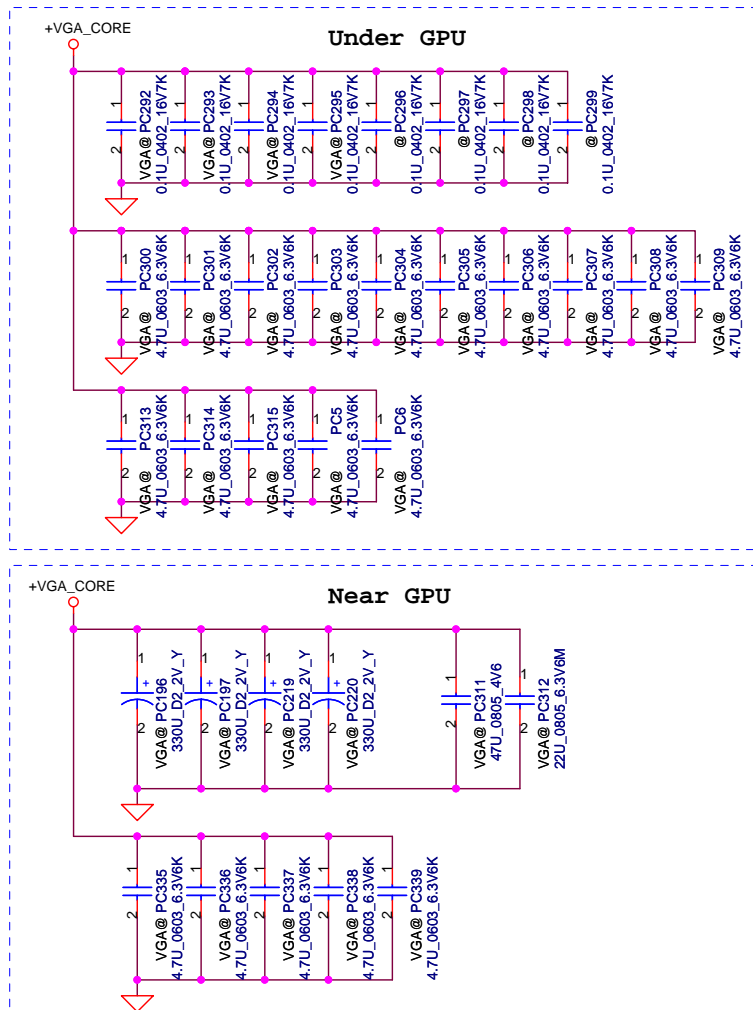




- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



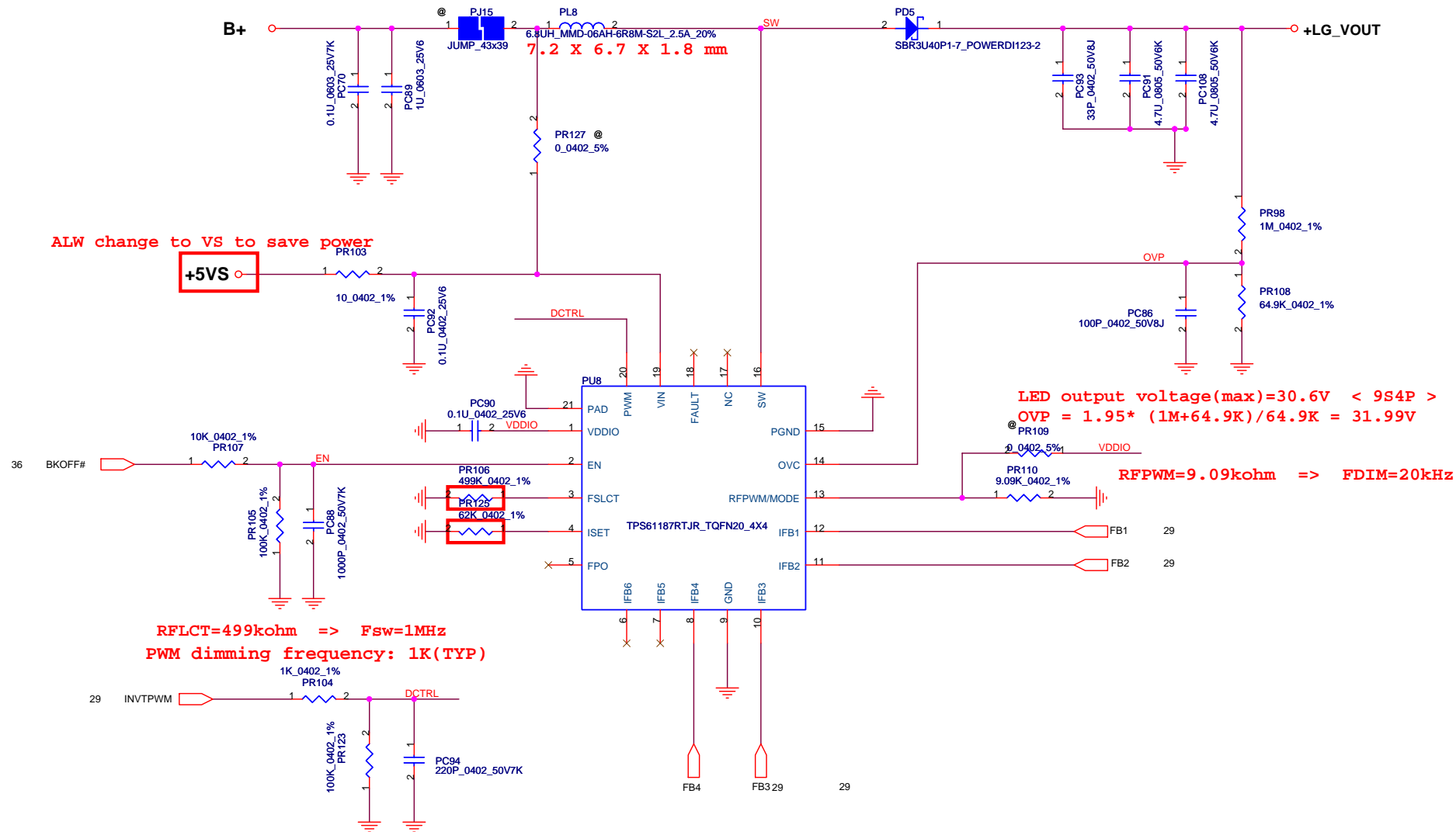
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NV DG NVVDD
N13P-GS GB4-128
4.7Ux15,0.1Ux8(4@) Under GPU
330Ux4 , 47Ux1,22Ux1,4.7Ux5 Near GPU

330u=> ESR=9m ohm

| | | | | | | |
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| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|---------------------------|---|------|------------|---|-------|-------|
| 1 | VGA boot voltage | Vboot Voltage can not allow to boot to 1.1V | | VGA | take off the PR212 | 11/22 | EVT2 |
| 2 | HW sequence | tune the correct sequence | | VGA | PR209 set to 100k ohm, PC107 set to 0.1u | 11/22 | EVT2 |
| 3 | HW sequence | tune the correct sequence | | 1.05 | put on the PQ27 | 11/20 | EVT2 |
| 4 | HW sequence | tune the correct sequence | | 1.8 | put on the PQ28 | 11/20 | EVT2 |
| 5 | HW sequence | tune the correct sequence | | 0.75 | put on the PR91 680k, PC325 0.1u, PQ26, PJ16 | 11/20 | EVT2 |
| 6 | CPU overshoot | in order to follow the intel spec to reduce the overshoot | | CPU | change the original 330u X3 to 330u + 560u | 11/25 | EVT2 |
| 7 | HW sequence | tune the correct sequence | | 1.5V | add PJ16 and PQ26 | 11/22 | EVT2 |
| 8 | Panel demand | change the cap 35V to 50V | | LED driver | change pc91 and pc108 to 50V cap | 11/28 | EVT2 |
| 9 | ME demand | can see the cap through the thermal hole | | CPU | take out the pc158 replace by pc159 | 3/13 | PVT |
| 10 | acoustic demand | can't pass acoustic acer spec | | CPU | add PC158 PC159 | 3/22 | PVT2 |
| 11 | component Vgs not satisfy | afraid Vgs is too small | | charger | change PQ8 material | 3/22 | PVT2 |
| 12 | 0ohm resister cost down | PPM request cost down | | | R_SHORT PR49, PR80, PR92, PR124, PR101, PR130, PR207, PR218, PR236, PR243 | 3/22 | PVT2 |
| 13 | | | | | | | |
| 14 | | | | | | | |
| 15 | | | | | | | |
| 16 | | | | | | | |
| 17 | | | | | | | |

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Change R558 to @(0_0402),C618(0.1U_0402) for AD_PID0
ADD R455 PH 4.7K_0402(SD028470180)(DISASSOCIATE#) <- ?K
ADD R454(@) (0_0402) for cost down BT power control
ADD R456 (0_0402)(SD028000080) for IOAC Pin46
POP Q46,R590 for Boardcom WLAN discharge

1/31
ADD R160 (0_0402) for USB_OC1# USB_OC0# colay

2/1
R549.1,R548.1 change from +3VLP to +3VALW_EC
remove stand along BT
remove USB20_N13 USB20_P13

for ESD:
ADD C416 0.1U_0402 ON/OFFBTN#
ADD C420 0.1U_0402 ON/OFF
ADD C421 0.1U_0402 BL_RESET
POP C345 0.01U_0402 PLT_RST#

Y2,X1 main source change from SJ10000DM00 to SJ100004Z00

2/2
ADD C151(@) 330U_D2
change U13 from SA00005AGE0 to SA00005AG00 (QS PCH)

2/6
ADD C91 @ 4.7U_0603 for WLAN Power CAP(SE107475K80)

2/7
for N13P-GS QS,MP strap
change R186 from 35K to 5K (Strap1 PD)

2/10
ADD Q43 (S TR AO3419L 1P SOT23-3) and JBL2 (S H-CONN ACES 50578-0040N-001 4P P1) for back light

2/13
for NV strap P.24
Change R184 from ES2GPU@ to @ (strap 2)
Delete R473 ES2GPU@ 10K_0402_1% (strap4)
Delete R469 HYN2G@ 34.8K_0402_1% (ROM_SCLK)
Add Hynix VRAM SA00004GD50 strap table (ROM_SI PD25K)

for Option Component
Delete PCB 8202@
Delete GPU U14 ES2GPU@ (SA000051800),QS2GPU@ (SA000051800)
Delete VRAM GDDR3@
Delete PCH U13 QSPCH@ (SA00005AG00),ES2PCH@ (SA00004NQB0)
Change VRAM X76 GDDR5@ to VRAM@ and add X76364BOL04

for PCH
Change U13 from SA00005AGE0 to SA00005AG00

for WLAN
Change R328,R455 from 4.7K_0402_5% to 10K_0402_5%
Change R73,R7,R102,R257,R279 from 0_0402_5% to 0 R_SHORT

2/14
for KB back light
Change location JBL2 to JBL1
Add Q26 (2N7002K_SOT23-3) and R318 510K_0402_5%

for GDDR5 GPIO define
Change R43 GDDR3@ to R43 @
Change R68 GDDR5@ to R68 DIS@

For GPU strap
Change R183 QSGPU@ to DIS@ (strap2)
Change R473 QSGPU@ to DIS@ (strap4)
Change R469 4.99K_0402_1% HYN2G@ to HYNMFR@ (ROM_SI)
Add R469 24.9K_0402_1% HYNAFR@ for VRAM Hynix AFR strap

2/15
for WLAN LED
Change EC pin102 net name from VCIN1_PROCHOT_R to IRST_RST# P.38
Add net IRST_RST_R# on U25 pin1 and link R162 0_0402_5% to IRST_RST# P.17
Add R161 0_0402_5% on PLT_RST# P.17
Add net name PLT_RST_R# between R161 and R10 P.17

for LAN
Change net name from PLT_RST# to PLT_RST_BUF# P.34
Add net name PLT_RST_BUF_R# between R149.2 and U62.2

for KB back light
Add net name GPXIOA07_R between Q43.2 and Q26.1
Change R559 18K_0402_5% to 33K_0402_5%

2/15A
L27 change main source from SHI00007400 to SH00000JM00
ADD R163(0_0402_5%) for PLT_RST_LAN#

2/16
R422,R619,R65 change to 0ohm-Rshort
C452 change from 15P to 18P
Chang JBL1 footprint from 抽屨式 SP01000ZW00 to 掀蓋式 SP01000Z300
SW1 change to unpop

02/17
Q45,Q46 2N7002 change to Q54 dual 2N7002
3VSWLAN_R change name to +3VS_WLAN_R trace 20mil

2/18
R34 unpop(SUSWARN# PH 10K)
R26 unpop(PCH_ACIN PH 10K)

2/21
R466 change from 5K to 10K(for device manager 3D device)

Rev1.0
3/14
ADD D21 ESD diode near ODD prevent PCH crack
Q1 Q4 2N7002 combine to Dual 2N7002 Q55
R559 change 33K to 56K_0402_5% SD028560280(for Board ID 4)
R318 change 510K to 100K (BL KB)

3/15
R415 R150,R278,R280,R291,R295,R298 ,R584,R86,R160 change 0_0402_5# ot Rshort_0402
R450,R497 0_0603_5% to Rshort_0603
ADD C552,C556,C558,C580,C581 for ESD
(BATT_AMB_LED#,BATT_BLUE_LED#,PWR_SUSP_LED#,PWR_LED#,+3VALW) Place near JLED1
Q3,Q16,Q17,Q19,Q44 change from SB501380020 to SB501380050 (HF)

3/22
change PCH to MP version to SA00005AGI0

4/5
CR CPU P/N change to MP PN
SA00005L5C0,SA00005K6B0,SA00005K5B0
remove Q50 for PROCHOT# connection issue
4/10
follow ESD suggest remove D28,D13 for cost down

Rev1A 4/10 Fix Q50 PROCHOT# connection issue

5/8
Change SA00005MX10 (S IC AV8062701048004 QAXQ J1 1.5G BGA) to SA00005MX60 (S IC AV8062701048004 SR0CW J1 1.5G ABO)
Rev1A 5/9 Change R559 from 56K to 100K(Board ID update)

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PCB

ZZZ



LA-8203P REV1 M/B
DAZ0O200100

LA-8203P MB Rev0: DA80000T600
LA-8203P MB Rev1: DA80000T610
LA-8203P MB with Small Board Rev1: DAZ0O200100

CPU

UCPU1



S IC AV8062701047904 SR0CV J1 1.4G ABO!
SA000051H60

AV8062701047904 SR0CV J1 1.4G ABO!

UCPU1



S IC AV8062701048004 SR0CW J1 1.5G ABO!
SA00005MX60

AV8062701048004 SR0CW J1 1.5G ABO!

UCPU1



S IC AV8062701047504 SR0D6 J1 1.6G ABO!
SA00004X010

AV8062701047504 SR0D6 J1 1.6G ABO!

SANDY BRIDGE

UCPU1



S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !
SA00005L5C0

AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !

UCPU1



S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0

AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1



S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !
SA00005K5B0

AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !

IVY BRIDGE

UCPU1



S IC AV8063801057401 QBP8 K0 1.5G BGA
SA00005AZ00

AV8063801057401 QBP8 K0 1.5G BGA

UCPU1



S IC AV8063801057400 QBP7 K0 1.7G BGA
SA00005B000

AV8063801057400 QBP7 K0 1.7G BGA

EVT2

VRAM

ZZZ



ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1
ALT. GROUP PARTS VRAMX4 HYN1G 38NM Q5LJ1
X76364BOL03|X76364BOL04

ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1

DRAM

ZZZ



ALT. GROUP PARTS DRAM X4 ELP 2G Q5LJ1
ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1
X76364BOL11|X76364BOL12

ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1

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